MS Diploma and Semester Projects offered at the Microelectronic Systems Laboratory during the winter 2018-2019

Students are asked to contact the project responsible to register. The majority of the projects are proposed as MS Diploma and Semester, and the amount of work will be adapted. Also, some projects can be carried out in groups of two students.

Projects are proposed in six categories in the following pages.
- Analog and mixed-signal circuits
- Digital circuits and modeling
- Bio-electronic interfaces and biomedical applications
- Fabrication technologies
- Industrial projects / external projects (for MSc diploma)
- Application development (software development)
Over the years, VLSI Systems-on-Chip (SoCs) and microprocessors have required an increasing amount of embedded memories in order to reach higher performances. According to the International Technology Roadmap for Semiconductors (ITRS), this trend will continue in the foreseeable future. The traditional type of embedded memory architecture has been the 6-transistor (6T) SRAM, which provides high-speed read and write performance with robust static data retention. However, due to the large 6-transistor bitcell and the large area peripheral circuit, most of the die of such implementation is occupied by the SRAM memory blocks. Besides, the off-transistor leakage currents in SRAM cells became one of the major power consuming components, in advanced technology nodes. An Application-specific Integrated Circuit (ASIC) containing such embedded memories has been recently developed in LSM (Fig.1) [1].

An interesting alternative to replace the SRAM, while continuing to provide full CMOS logic compatibility, is the logic compatible Gain Cell embedded DRAM (GC eDRAM) arrays that present higher density, lower power consumption, higher reliability and 2-port functionality in advanced nodes [2] (Fig. 2). However, the data retention of GC-eDRAMs depends on dynamically stored charge, which thereby needs periodic and power hungry refresh operations.

The goal of this master project is to design and implement a Gain-cell embedded DRAM macro targeting high-density and low-power performances in an advanced technology node (28nm CMOS), in order to be used as an alternative on-chip memory in our future ASIC designs. Firstly, the student will acquire the necessary knowledge about the state-of-the-art of GC eDRAM. Based on this, he will design and implement the proper bitcell topologies using Cadence and select the most suitable one in terms of power, density and retention time. Then, a memory macro including the read and write circuits will be implemented. Finally, the full system will be simulated and tested.

<table>
<thead>
<tr>
<th>A1</th>
<th>System Design and Implementation of Gain-Cell eDRAM in 28nm CMOS technology</th>
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<tr>
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Master project

Project breakdown:
20% Literature review  
40% Schematic design and simulation  
40% Layout design

Supervisors in charge:  
Jonathan Narinx (jonathan.narinx@epfl.ch)  
Responsible teacher: Prof. Yusuf Leblebici

A2 Implementation of a new high speed Analog-to-Digital Converter (ADC) based on a pipelined – threshold Configuring SAR architecture

The demand on high speed ADCs (>10GS/s) have consequently increased over the years with the development of new communication standards, oscilloscopes, or 5G network. These high sampling rates are obtained usually by time-interleaving several channels. However, each sub ADC should itself operate at a maximum speed with acceptable power consumption in order to limit the total number of interleaved channels.

In this project, the student will explore a new architecture enabling very high sampling rate for a Successive Approximation (SAR) ADC. He/She will combine threshold-configuring technique with standard SAR architecture in a pipelined manner, so that the final sampling rate could reach 1.5GS/s for 8-bit resolution. A previous work has already been done on this architecture at schematic level, so the student will focus on the layout and post-layout simulations. He/she will work with state-of-the-art 28nm FD-SOI technology.

Effort Breakdown:  
10 % Literature review.  
30% Schematics and simulation.  
60% Layout and Post-layout Simulations.

Contact/Supervisor in charge: Mustafa Kilic (mustafa.kilic@epfl.ch)  
Responsible Professor: Yusuf Leblebici

A3 Implementation of dynamic element matching technique in high speed SAR ADCs to correct capacitor mismatch-due non-linearity

Recent ADCs, whatever its architecture, usually requires a capacitive DAC in it. Mismatch between the capacitor elements usually causes non-linearity issues when the resolution is higher than 10 bit. In some applications such as signal detection, ADC linearity is more important than its noise level. Dynamic element matching is a technique enabling to convert the mismatch-due distortion spurs into a white noise. However, due to the high number of capacitor cells in a >10b ADC, it was hard to apply this technique for high speed and low power/ low area SAR ADCs.

In this project, the student will discover a new technique aiming at applying dynamic element matching technique suitable for high-speed architectures. HE will implement the different blocks that constitute the ADC from schematic to layout.

Effort Breakdown:  
10 % Literature review.  
40% Schematic simulation.  
50% Layout and Post layout simulation.

Contact/Supervisor in charge: Mustafa Kilic (mustafa.kilic@epfl.ch)  
Responsible Professor: Yusuf Leblebici

A4 Design and study of a new front-end architecture for Time-interleaved Analog-to-Digital Converters (ADC)

Time Interleaved architectures are based on running several ADC in parallel with a time shift in order to obtain a very high sampling rate (usually >10GSPS). However the clock jitter becomes an important issue at when sampling high frequency signals, limiting the overall ADC performances. In this project, the student will study an ADC architecture that has several input switches that may
average the clock jitter at the sampling phase. If the overall clock noise is reduced, higher resolutions may be obtained at high sampling rates from the TI-ADC. The student will first modelize the input front-end of the Time-interleaved ADC and see the jitter averaging effect. Then he will implement the input signal distribution and simulate full TI-ADC performances using advanced CMOS technology.

20 % Literature review.
30 % Matlab/Verilog-a Models.
50% Layout and post-layout simulation.

Contact/Supervisor in charge: Mustafa Kilic (mustafa.kilic@epfl.ch)
Responsible Professor: Yusuf Leblebici

<table>
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<tr>
<th>A5</th>
<th>Implementation of a calibration structure for a 64-channel, 50 GS/s time-interleaved analog-to-digital converter (TI-ADC) in 28nm FD-SOI process</th>
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<td>Time-interleaving is a commonly resorted solution to linearize the power-speed trade-off for high throughput ADCs. This technique employs multiple ADCs in parallel instead of increasing the sampling clock frequency. Utilizing more than one ADC brings another constraint to the trade-off polygon, which is inter-channel mismatch. Critical parameters such as offset, gain, and sampling time of the sub-ADCs may vary substantially from channel to channel. Independent of the quality of a sub-ADC, these mismatches have detrimental effects on the performance of the overall TI-ADC. However, it is possible to tolerate mismatch and to mitigate its causes and/or effects using on-chip calibration structures. The goal of this project is to implement an on-chip calibration structure to recover the inter-channel mismatch effects in a 64-channel, 50 GS/s time-interleaved analog-to-digital converter. The student is expected first to understand the current calibration solutions, model them in Matlab environment, and then realize the model on silicon.</td>
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<td>Project cutdown: 10% Literature study 10% Matlab modeling 30% Semi-custom design and verification of calibration processor 20% Full-custom design of the peripherals and block integration 30% Layout design</td>
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<td>Project for 1 MSc diploma student</td>
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<td>Supervisors: Arda Uran (<a href="mailto:arda.uran@epfl.ch">arda.uran@epfl.ch</a>) Mustafa Kilic (<a href="mailto:mustafa.kilic@epfl.ch">mustafa.kilic@epfl.ch</a>)</td>
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<td>Responsible Professor: Yusuf Leblebici</td>
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| A6 | (void) |
Wireless implantable devices capable of monitoring the brain’s activity are becoming an important tool for understanding mental diseases and potentially restore motor functions due to central nervous system disorders, such as spinal cord injury. Our current research is to exploit the structure of intracranial electroencephalogram (iEEG) signals to reduce power consumption associated to the transmission of data from an implantable device in the human cortex to a second device, implanted in the spinal cord. To this end, innovative machine learning based approaches, are used to design very efficient data encoders on hardware, which are signal-structure aware (Fig. 1). With this premise in mind, we can significantly improve the encoder-decoder combination, tailoring their design to boost the overall system performance. A neural network system (Fig. 2) exploits the signal structure and enhance the performance of the macro, by using minor assumptions on the signal of interest.

The project results have great potentials to become a milestone for future work, targeting publications in different domains.

Project goal: Hardware implementation of the neural-network based decoder.

Project breakdown:
- 20% Literature review
- 20% Matlab algorithm study and development
- 40% Semi-custom digital design
- 20% Frontend full-custom design and simulations

Supervisors in charge:
Arda Uran (arda.uran@epfl.ch)
Prof. Yusuf Leblebici (LSM)
Prof. Volkan Cevher (Lions@epfl)

D2 (void)
D3 (void)
D4 Hardware/software co-design of a complete real-time video processing system using the Xilinx Zynq UltraScale+ MPSoC ZCU102 Development Board
The goal of this project is to implement a complete real-time video processing system using the new Xilinx ZCU102 Evaluation Board (Fig. 1). This board features a Zynq UltraScale+™ MPSoC device with a quad-core ARM® Cortex-A53, dual-core Cortex-R5 real-time processors, and a Mali-400 MP2 graphics processing unit based on Xilinx's 16nm FinFET+ programmable logic fabric (Fig. 2).

The video processing system will consist of interfacing two or three high-resolution cameras from the USB-3 or MIPI interface, processing the video streams using the Zynq UltraScale+™ MPSoC, and output the results using the HDMI or USB-3 interface. The video processing task will be based on enhancement of the panorama stitching algorithm by utilizing the depth map estimation hardware developed at LSM.

Depending on the performance of the full system, the student will have to choose which parts to implement in the Processing System (PS) or to accelerate using the Programmable Logic (PL) to make the system real-time.

Master project

Project breakdown:
10% Literature review
40% Hardware design (Xilinx Vivado, Vivado HLS)
50% Software design (Xilinx SDSoC)

Supervisors in charge:
Jonathan Narinx (jonathan.narinx@epfl.ch)
Responsible teacher: Prof. Yusuf Leblebici

Further readings:
https://www.xilinx.com/products/design-tools/embedded-vision-zone.html
http://www.wiki.xilinx.com/reVISION%2BGetting%2BStarted%2BGuide%2B2017.2

D5 Efficient Hardware Implementation of a Real-Time Depth Map Filtering Solution

With the increasing prominence of real-time streaming video platforms, the demand for high-quality and real-time depth imaging devices has considerably increased in a wide variety of video processing applications where the 3D information has become essential, such as in autonomous vehicles, robotics, Virtual Reality (VR), etc. Depth estimation can be performed by exploiting different techniques, e.g. structured light projection, Time-of-Flight (ToF) or Disparity Estimation (DE) using stereo cameras. Unlike other techniques, DE is based only on passive image sensors, which enable high-resolution depth maps at low-power, even in outdoor conditions (direct sunlight), and without any interference with other systems. Furthermore, the depth map quality of binocular configuration
can be enhanced by using additional cameras, which prevent most of the erroneous depth estimations due to occluded areas. However, the major drawback of DE is the erroneous disparity computations that comes from the stereo-matching process. Indeed, repetitive texture or textureless areas lead usually to some ambiguity during the pixel correspondence process, which results in wrongly computed disparity values (Fig. 1). Furthermore, occluded areas will also lead to errors in the final depth map, especially in binocular configurations.

The goal of this project is to develop a hardware-based filtering solution to reduce the noise of the depth maps obtained from a novel trinocular real-time disparity estimation system recently developed in LSM [1]. The hardware should be able to process in real-time (> 60 fps) 2K resolution images and provide a sufficient good filtering performance. Moreover the hardware should be efficient in terms of hardware resources utilization.

In this project, the student will first acquire the necessary knowledge about the state-of-the-art hardware implementation of disparity estimation and their filtering solutions (median, bilateral, Gaussian, etc.). Based on this, he will develop an efficient hardware oriented implementation of the chosen filtering algorithm on MATLAB and then, its HDL coding will be performed. The hardware will be implemented and simulated on ModelSim, and then tested on a FPGA Virtex-7 development board using Xilinx Design Tools.

![RGB image and depth map of a scene](image)

Figure 1: RGB image and depth map of a scene [1].


Project breakdown:
- 20% Literature review
- 30% MATLAB implementation
- 60% ModelSim simulation & FPGA implementation

Supervisors in charge:
- Bilal Demir (bilal.demir@epfl.ch)
- Jonathan Narinx (jonathan.narinx@epfl.ch)

Responsible teacher: Prof. Yusuf Leblebici
**Bio-electronic interfaces and biomedical applications**

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<td>B2</td>
<td><strong>Epilepsy Feature Extraction Using Support Vector Machine (SVM)</strong></td>
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Machine learning is the study of pattern recognition and computational learning theory in artificial intelligence. It has different applications such as finance, E-commerce, web-search, space exploration, robotics, etc.

In this project, our goal is to detect the epilepsy by means of a supervised learning which is defined as a type of learning that the computer is presented with example inputs and their desired outputs, given by a "teacher", and the goal is to learn a general rule that maps inputs to outputs. The student should be able to:
1) Implement the SVM on the FPGA.
2) Implement the SVM using 0.18 um technology.

Project cut-down:
- 20% literature review
- 25% FPGA programming
- 20% Design and simulation using 0.18 um UMC
- 35% Full-custom layout using 0.18 um UMC

contact person: Reza Ranjandish (reza.ranjandish@epfl.ch)
Responsible Professor: Alexandre Schmid

| B3 | - |
# Fabrication Technologies

## N1 Fabrication and characterization of ReRAM crossbars

Memories are intricate part of most of integrated circuits, the popular consumer products in the mass storage space made memory devices as the most common transistors in the market nowadays.

It is becoming increasingly more challenging to continue the current pace of scaling down the conventional technologies as they are charge based and are facing physical limitation in further shrinking in their size, while it is highly demanded by the industry. Therefore, new memory candidates are emerged and been studied extensively in the last decade. Resistive Random Access Memories (ReRAMs/RRAMs) are considered as one of the most promising candidates with a proper trade-off between desired parameters such as: low cost of fabrication, nonvolatility, Speed, Endurance, Retention and Power consumption. The concept is easy and straightforward, an insulator layer is sandwiched between two metal layers. For many device types the exact mechanisms that cause the change in resistance state is not well known, but they are known to occur in the bulk of the insulator layer, along some conducting filaments, or at the insulator-metal interface. Depending on the material system, the set/reset processes can be carried out in bipolar or unipolar voltage polarity.

The objective of this project is to design, fabricate and electrically characterized the devices, from single cell to array level. In this project, the student will start with designing and fabrication a single cell device(stand-alone memory), the device fabricated stand-alone device with the best performance will be implemented for array level(crossbar). The students beside having the opportunity of working with state of the art equipment (Ebeam, SEM, …) will have the opportunity to measure synaptic behavior (STDP,…) of the fabricated array device for neuromorphic applications.

Work description:
- 10% literature review,
- 60% fabrication,
- 30% Electrical /material characterizations,

Fabrication will be done in CMI cleanroom (BM building) of EPFL and it requires training for having access to the needed equipment.

Type of Project: Master Project/ Semester Project

Contact: Behnoush attari (Behnoush.attarimashalkoubeh@epfl.ch)
Supervisor: Y. Leblebici

## N2 Uniformity and reliability improvement of resistive switching of Resistive Random Access memory(ReRAM)

Resistive Random Access Memories (ReRAMs/RRAMs) are considered as one of the most promising candidates with a proper trade-off between desired parameters such as: low cost of fabrication, nonvolatility, Speed, Endurance, Retention and Power consumption. The concept is easy and straightforward, an insulator layer is sandwiched between two metal layers. For many device types the exact mechanisms that cause the change in resistance state is not well known, but they are known to occur in the bulk of the insulator layer, along some conducting filaments, or at the insulator-metal interface.

The objective of this project is to design, fabricate and electrically characterized ReRAM devices in order to achieve a device with a proper tradeoff between key switching parameters and reliability.

Work description:
- 10% literature review,
- 60% fabrication,
- 30% Electrical and material characterizations,
Fabrication will be done in CMI cleanroom (BM building) of EPFL and it requires training for having access to the needed equipment.

Type of Project: Semester Project

Contact: Behnoush attari (Behnoush.attarimashalkoubeh@epfl.ch)
Supervisor: Y. Leblebici

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### Industrial projects / External projects (MSc diploma)

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<thead>
<tr>
<th>IE1</th>
<th>EM Microelectronic</th>
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<tr>
<td></td>
<td>is proposing a number of internships that could be of interest for EE/CS students in your organization. The topics can be found at the link below and we would very much appreciate if you could help inform your students regarding these opportunities. Internships can potentially and in agreement with the student and his thesis advisor be extended into a M.Sc. thesis project.</td>
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<td><a href="http://www.emmicroelectronic.com/jobs">http://www.emmicroelectronic.com/jobs</a></td>
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<td>Interested students should submit application letter and resume (CV) as soon as possible: <a href="mailto:Recruiting@emmicroelectronic.com">Recruiting@emmicroelectronic.com</a></td>
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<tr>
<td></td>
<td>As an EPFL registered internship or MSc diploma, please also contact one of the following possible supervisor: Y. Leblebici, A. Vachoux, A. Schmid</td>
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**Application development (software development)**

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