Acknowledgements

First of all, I would like thank Prof. Yusuf Leblebici not only for giving me the opportunity to work on my master thesis at LSM, but also for the support he has given as research scholarship.

I also would like to thank Tuğba Demirci for her supervision. She has shared her valuable experiences with me and always helped me about both my technical and daily problems.

Moreover, I would like to express my appreciation to Armin Tajalli for his helpful recommendations and sparing his valuable time.

Furthermore, I want to thank Ayça Akkaya for her endless support in every aspect of my life.

I also want to thank Duygu and Arda from LSM for their friendship. Also I am grateful to all the other friends in Lausanne and hoping that this friendship will last very long.

Finally, I want to express my gratitude to my family for their love, encouragement and everything that helped me for being who I am today.
Abstract

CMOS scaling has enabled significant advances in operating frequencies of integrated circuits, whereas the data rates of chip-to-chip communication systems have not improved accordingly. These developments lead to high demand on high speed transmitter and receiver circuits. Moreover, JESD204B is a new serial communication standard that offers many advantages for multi-channel data converter systems. Using JESD204B compliant transmitter could be very efficient to transfer the output signals of a 64-channel ADC system.

In this work, a transmitter circuit which is JESD204B standard compliant is designed in 28 nm FD-SOI technology working at 1V power supply. Since 8-bit/10-bit encoding technique is used, 10-to-1 D flip-flop based serializer and current mode push-pull type transmitter topologies are selected. To fulfill the reflection specifications, double termination has been planned in the system. Also, AC coupling mode is planned to be used because of the common mode specifications of the receiver side. At the end, 12.5 Gbps data rate is achieved with the voltage swing that is defined in the electrical specifications of the standard.

Keywords

JESD204B, serial communication, high speed electrical link, serializer, transmitter.
Contents

Acknowledgements ........................................................................................................... i
Abstract ............................................................................................................................ iii
Keywords ........................................................................................................................... iii
Contents ......................................................................................................................... v
List of Figures ................................................................................................................... vii
List of Tables ................................................................................................................... ix

Chapter 1 Introduction ................................................................................................. 1
  1.1 Advantages of Time Interleaved ADCs ................................................................. 1
  1.2 General Information about the System ............................................................... 4

Chapter 2 Background Information .......................................................................... 7
  2.1 Serial Communication ......................................................................................... 7
  2.2 JESD204B Standard ............................................................................................. 8
  2.3 Termination ........................................................................................................... 9
  2.4 Serializer ............................................................................................................. 11
    2.4.1 Multiplexer Based Serializer ....................................................................... 11
    2.4.2 D Flip-Flop Based Serializer ...................................................................... 13
  2.5 Transmitter ......................................................................................................... 14
    2.5.1 Single Ended vs. Differential Transmitter ..................................................... 14
    2.5.2 Voltage Mode vs. Current Mode Transmitter ................................................ 15
    2.5.3 Push-Pull vs. Pull-Only Transmitter ............................................................ 16

Chapter 3 Design ....................................................................................................... 19
  3.1 Design Specifications ......................................................................................... 19
  3.2 Serializer Design .................................................................................................. 20
  3.3 Transmitter and Its Building Blocks .................................................................... 24
    3.3.1 Transmitter Design ....................................................................................... 24
    3.3.2 Current Source Design ................................................................................ 26
3.3.3 Operational Transconductance Amplifier Design ........................................ 27
3.3.4 Common Mode Feedback ........................................................................... 30
3.4 Modeling of PCB Trace .................................................................................. 31
3.5 Top Level Simulation Results ......................................................................... 34
Chapter 4 Tape-Out Work ..................................................................................... 39
Chapter 5 Conclusion ............................................................................................ 41
  5.1 Achieved Results ......................................................................................... 41
  5.2 Future Development ..................................................................................... 41
References ........................................................................................................... 43
List of Figures

Figure 1.1 Time Interleaving Principle ......................................................... 2
Figure 1.2 Sampling in 4 Channel ADC .......................................................... 2
Figure 1.3 SNDR and Sampling Rate Plot of Different ADC Types ............... 3
Figure 1.4 Block Diagram of the System ....................................................... 4
Figure 2.1 High Speed Electrical Link System .............................................. 9
Figure 2.2 Series Termination (a) Parallel Termination (b) ......................... 10
Figure 2.3 Full Rate MUX Based Serializer Structure ................................ 12
Figure 2.4 Half Rate MUX Based Serializer Structure ................................ 12
Figure 2.5 D Flip-Flop Based Serializer Structure ...................................... 13
Figure 2.6 Single Ended (a) and Differential (b) Transmitter Examples ....... 14
Figure 2.7 Voltage Mode Transmitter Example ............................................. 15
Figure 2.8 Push-Pull (a) and Pull-Only (b) Transmitters .......................... 16
Figure 3.1 Designed Serializer Circuit ....................................................... 21
Figure 3.2 Load Generator Circuit .............................................................. 22
Figure 3.3 Load Signal Generation Waveforms .......................................... 22
Figure 3.4 Output Waveform of the Serializer for the Input = 1010101010 .............................................................. 23
Figure 3.5 The Layout of the Serializer ...................................................... 24
Figure 3.6 Transmitter Design ................................................................. 25
Figure 3.7 The Layout of the Transmitter .................................................... 26
Figure 3.8 OTA Design .............................................................................. 28
Figure 3.9 Gain and Phase Plot of the OTA ................................................. 29
Figure 3.10 Offset Value Histogram ........................................................... 29
Figure 3.11 The Layout of the OTA ............................................................ 30
Figure 3.12 Gain Phase Plot of the CMFB .................................................. 31
Figure 3.13 Cross Section of a Microstrip Line ......................................... 32
Figure 3.14 S-Parameters of 100mm Line .................................................. 33
Figure 3.15 S-Parameters of 40mm Line ..................................................... 33
Figure 3.16 Cross Section of a Microstrip Coupled Line..........................34
Figure 3.17 S11 of the Transmitter......................................................35
Figure 3.18 Eye Diagram for 40mm Line .............................................36
Figure 3.19 Eye Diagram for 100mm Line .............................................36
Figure 3.20 Eye Diagram of Four Different Channels ..............................37
Figure 4.1 The Layout of the Tape-Out Work........................................39
List of Tables

Table 2.1 Pin Count Comparison for 12 Bit ADC..................................................8
Table 3.1 JESD204B Standard Transmitter Electrical Specifications...........20
Table 3.2 Threshold Values for Different Bulk Voltages.........................25
Table 3.3 Corner Simulation Results of NMOS Current Source...............27
Table 3.4 Corner Simulation Results of PMOS Current Source .............27
Table 3.5 Corner Simulation Results of the OTA .....................................29
Table 3.6 Parameters of 100 mm Line for FR-4.......................................32
Chapter 1  Introduction

As the sampling rates of the analog to digital converters (ADCs) increase, the limitation on the number of pins becomes an important issue for integrated circuits. Low voltage differential signaling (LVDS) interface has almost completely overtaken the complementary metal oxide semiconductor (CMOS) interface in high-speed applications. However, actual decrease in the number of pins has been reached with serial communication interfaces such as serial LVDS. JESD204B is a relatively new serial communication standard that supports much faster data rates and has many important features especially for multi-channel analog to digital converter systems.

In this project, a transmitter which is compliant to JESD204B standard will be designed for 64-channel ADC system. Information about the advantages of time interleaved ADCs and the ADC system that the transmitter is used in will be given to explain the purpose of the circuit better.

1.1  Advantages of Time Interleaved ADCs

Analog to digital converters substantially limit the performances of most of the communication systems today. Therefore, these systems constantly push for higher sampling rates and resolution. Maybe the most recent example is 100Gbit/s Ethernet standard IEEE 802.3bj. This standard requires ADCs that have 5 effective number of bits (ENOB). Another standard requires 10Gbps bit rate but its ENOB specification is 5-6 bit [1]. Moreover, instrumentation and oscilloscope could be given as another application example. It requires 20GS/s to 30GS/s sampling frequency with 7-8 bit ENOB.

Time interleaving is a method that combines more than one identical N-bit ADCs to reach higher sampling rates. Its working principle is that to reach fs sampling frequency, relatively slow M ADCs, whose sampling frequency is fs/M each, can be used in parallel as it is shown in Figure 1.1. Each ADC samples the input signal once in every M/fs seconds and these ADCs are multiplexed in time. First ADC will sample the input signal and convert it to digital output. 1/fs seconds later the second ADC starts conversion and so on. The digital bits at the output are also multiplexed in the same way the ADCs are chosen. In the end, what we have in a black box is an ADC with N-bit resolution and fs sampling rate.
Moreover, the speed advantage also creates wider Nyquist zone. In other words, with increased sampling rate, it is possible to convert the signals which have higher frequency components and this is very useful for many communication systems. In Figure 1.2 it is shown how four different channels are sampling the same sinusoidal input signal. It can easily be seen that the more ADC channels are used, the higher Nyquist frequency can be achieved.

Although time interleaved ADCs are mentioned as being advantageous in sampling rate while disadvantageous in power consumption and area when it was first published in 1980 [2], it has many other benefits that were discovered later [3]. First of all, the speed of a single channel ADC is determined by the speed of sampler and quantizer together. But sampler's performance mostly limits the maximum number of time interleaved channel because the time constant of the sampler determines the bandwidth of the input signal. Since M times slower sub ADCs are used, specifications for sampling phase such as sampling interval are much relaxed; therefore, this means with a good design of sampler such as using bootstrapping technique very major improvement in the maximum sampling speed can be reached.
Secondly, one of the most important advantages of time interleaving technique whose importance is not realized for years is positive effect in the power speed tradeoff. Thanks to this advantage, especially recent works on successive approximation register ADCs (SAR ADCs) have achieved very good SNDR and fs values as shown in Figure 1.3 [4] [5].

Interleaving improves figure of merit significantly because when conversion speed of a single channel ADC gets close to the technological limits, the circuit starts to need more power for the certain amount of speed improvement. As an example, increment rate of comparator speed decreases as we increase its power consumption. Thus, the power-speed tradeoff becomes nonlinear. Consequently, it is possible to reach much better figure of merits by using time interleaving technique because of its linear power-speed relation.

Finally, M-channel time interleaved ADC needs delay locked loop (DLL) or phase locked loop (PLL) for its clock phases which are uniformly separated. To distribute these clock signals properly, it is needed to have a clock network. Another advantage of time interleaving is that it can decrease the power consumption of clock distribution network because when more than one channel is used, it can be tolerated to have more delay in clock distribution buffers, compared to single channel ADC running at the same sampling rate. Therefore, buffer transistors can be designed smaller which can decrease the MOS switch capacitance, which leads to less dynamic power consumption.

![Figure 1.3 SNDR and Sampling Rate Plot of Different ADC Types](image-url)
1.2 General Information about the System

We are planning to have a high speed and moderate resolution ADC system and to do so, we have aimed to design 10-bit 64-channel time interleaved SAR ADC architecture. Advantages of SAR ADCs are mentioned in the previous section. To fulfill the specifications of this ADC system we need to have a phase locked loop with LC type voltage controlled oscillator. This phase locked loop generates clean 12GHz clock signal for more than one circuit.

First of all, this clean 12 GHz clock signal is the input of a delay locked loop circuit which is responsible for generating different clock phases. Delay locked loop is a circuit that allows us to lock an input signal and create different phases of this signal thanks to its delay line structure. For a time interleaved ADC, it is essential to have different phases of the clock signal for different channels because each ADC channel needs to sample the input signal one by one and these sample signal phases must uniformly span 360 degrees. Each delay locked loop is responsible for generating four clock phases which are 0, 90, 180 and 270 degrees and each of these clock signals will be the sampling signals of four different ADCs. There is no need to route any other signal but the sampling signal because it is planned to have asynchronous ADCs which only need a sampling signal. All other clock signals inside single channel ADC are generated from the sampling signal; thus, asynchronous ADC structure does not need an additional clock signal.

![Figure 1.4 Block Diagram of the System](image-url)
Secondly, the clean clock that is generated by phase locked loop will be the input of JESD204B protocol logic block. However, this block needs many different clock frequencies. Therefore, we are planning to have clock divider circuits to generate all different clock frequencies that is needed for JESD204B logic block. Since JESD204B is a serial communication protocol we need a serializer and this serializer also requires different clock frequencies. But fortunately, all the clock frequencies that are needed by the serializer will also be needed by the JESD204B block; therefore, we could use the same clock signals also for the serializer. After that, we need to design a transmitter which is JESD204B compliant. To claim this compliance, the data rate should be 12.5 Gbps and the other electrical specifications should also be designed accordingly. Moreover, although the JESD204B standard supports data rate up to 12.5 Gbps, data rate is not limited to this value because most of the FPGAs which will be the receiver side of our serial communication claim to reach higher data rates for the same standard.

The block diagram of the system shown in Figure 1.4 is only a part of the whole system. This circuitry will be used 16 times in the overall system in order to achieve 64-channel time interleaved ADC architecture. For each 16 cells, the same PLL will be used for synchronization.
Chapter 2  Background Information

In this chapter general background information will be given about the project. To do so, advantages of serial communication will be discussed first. Then JESD204B standard, its evolution, predecessor revisions and advantages will be introduced. Then, theoretical information will be given about termination, serializer circuits and transmitter circuits respectively. All the information that is given in this chapter and the next chapters is especially targeted to be instructive.

2.1  Serial Communication

Digital data transfer can be done in two different modes which are parallel and series. In parallel transmission, several bits are transferred at the same time using different channels. These bits must be synchronized to each other and a clock signal. Therefore, parallel transmission needs wide data buses compared to serial transmission. In serial transmission, data is sent one bit at a time sequentially. Despite the fact that serial link transmits less data in each clock cycle, it is considered to be faster than parallel mode because of some reasons.

First of all, synchronization is a huge problem in parallel transmission since parallel data bits are needed to be read at the same time in the receiver side. To be sure that receiver reads the correct data bits, the transmission speed cannot be so high. However, this data skew or clock skew problem does not exist in serial mode.

Parallel LVDS interface has overtaken parallel CMOS interface in time because power consumption is something that we should consider along with the speed specification. In parallel CMOS interface, while data rate increases, power consumption also increases. For parallel LVDS interface power consumption does not change with the data rate and this is mainly because of the driver architecture. However, if we compare these parallel interfaces with a series one, it can be seen that serial interface requires much less pins. This is maybe the most useful advantage of serial communication.
<table>
<thead>
<tr>
<th>Number of Channels</th>
<th>Parallel Interface Number of Pins</th>
<th>Series Interface Number of Pins</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>13</td>
<td>2</td>
</tr>
<tr>
<td>2</td>
<td>26</td>
<td>4</td>
</tr>
<tr>
<td>4</td>
<td>52</td>
<td>8</td>
</tr>
<tr>
<td>8</td>
<td>104</td>
<td>16</td>
</tr>
</tbody>
</table>

Table 2.1 Pin Count Comparison for 12 Bit ADC

Table 2.1 compares the pin numbers of parallel CMOS interface with the series interface that has differential output, which is what we planned in our project, for different number of channels. High number of pins comes with high area penalty and increases the cost of the chip. Another disadvantage of high number of pins for an integrated circuit is that the complexity in printed circuit board (PCB) is much higher.

### 2.2 JESD204B Standard

JESD204 is a new converter interface standard whose first version was released in April 2006 but has got some updates to make it more suitable for data converter interfaces. Since speed and resolution of data converters have significantly increased in time, previous interfaces such as CMOS and LVDS have become inadequate. Two main reasons to prefer JESD204 interface are that it is a much faster interface which allows having data converters with high sampling rates and it has much lower number of pins that leads to smaller package size and less complex board design. Of course all of these reasons are very efficient to decrease the total cost of the system. JESD204 standard has already got two revisions which are JESD204A and JESD204B to fulfill the expectations of designers in terms of multi-channel data converters. In the next part, features of the revisions will be mentioned [6].

The first version of the standard which is JESD204 offers a serial link between one or more than one converters and field programmable gate array (FPGA) or application specific integrated circuit (ASIC) which is used as a receiver. Converters and the receiver use the same clock signal and the speed of the differential serial link is defined between 312.5 Mbps and 3.125 Gbps. The nominal peak to peak differential voltage is 800 mV and common mode voltage limit is between 720 mV and 1.23V. Also, to decrease the complexity and not to send the high speed clock signal with the data, 8b/10b encoding is used. By this means, clock recovery system can easily extract the clock signal of the data stream in the receiver side. A revision was needed to make the standard more suitable for multiple channel data converters with higher speed and resolution.

First revision of JESD204 is published in April 2008 and is named as JESD204A. In this version, bit rate, frame clock and the other electrical specifications remained the same. As a new feature, multiple aligned links for multiple data converters is added. Increased efficiency of the multiple aligned serial lanes eased to meet the maximum data rate which is 3.125 Gbps for high speed data converters. In this revision, what was still missing is the
deterministic latency information which is the timing relation between analog input signal and its digital output for an ADC. Lack of this deterministic latency of the converter and increase in sampling rates of the converters are the motivations for the second revision.

The last revision of the standard which is JESD204B has been released in July 2011. Compared to the other two versions, this version has the deterministic latency information of the converter and its serialized output. Moreover, JESD204B revision has increased the data rate support up to 12.5 Gbps. Differential source and load impedance is 100 Ω which is the same for all the versions. However, in JESD204B version of the standard, the data rate is divided into three different sections. The first section defines the lane data rate up to 3.125 Gbps and the second section defines the lane data rate up to 6.375 Gbps. In this second section, peak to peak differential voltage level is decreased from 500 mV to 400 mV. The third and the last speed section defines the lane data rate up to 12.5 Gbps and the minimum peak to peak differential voltage is 360 mV; therefore, this reduction in voltage leads to design transceivers with high data rates easier. Moreover, another change in this revision is that the device clock signals are used to reduce unnecessary complexities. In previous revisions, frame clock is used which means sampling clock of the converter and the clock signal of the receiver were the same but routing of the same frame clock signal to multiple devices could be difficult. However, in JESD204B, each device uses its own device clock as a reference and these reference clocks are created by a clock generator that generates all the device clocks from the same source.

2.3 Termination

General structure of high speed electrical link system is shown in Figure 2.1. One of the essential specifications of the system is the termination impedance. Most of the high performance serial link systems uses this specification in both transmitter and receiver side to boost the performance.

![Figure 2.1 High Speed Electrical Link System](image)

If a signal that passes through a transmission line come across a different characteristic impedance in the line, it can be partly or totally reflected back to reverse direction. This situation occurs if the load impedance does not match the characteristic impedance of the line. Reflection coefficient is defined as the ratio of the amplitude of the reflected wave to the amplitude of the incident wave. Therefore, if a transmission line is properly terminat-
ed with a load impedance which has the same impedance as the characteristic impedance of the line, the reflection coefficient will be zero.

\[
\text{Reflection Coefficient } \Gamma = \frac{Z_L - Z_0}{Z_L + Z_0}
\]

\[
V_{\text{reflected}} = \Gamma \cdot V_{\text{incident}}
\]

In this section, different termination types and their properties will be examined. First of all, series and parallel termination topics will be discussed. There are two types of drivers which will be examined later in detail. These types are voltage mode driver and current mode driver. Due to the circuit structure, voltage mode drivers have low -ideally zero- output impedance that forces to use series termination typically. On the contrary, current mode drivers have high output impedance -ideally infinite- and this type of drivers usually use parallel termination. The aim of this is to provide impedance matching that we have discussed before. At the end of the channel the impedance should be the same as the characteristic impedance of the channel. General structure of series and parallel termination is shown in Figure 2.2.

![Series Termination](a)
![Parallel Termination](b)

Figure 2.2 Series Termination (a) Parallel Termination (b)

Another consideration is that if the termination is done only on source side this is called source termination. Similarly, the line can also be terminated only on load side which is called load termination. In both cases, the ringing problem should be removed. For source termination, the reflection coefficient on the source side will be zero but on the load side it will be close to 1. If the driver has an output impedance other than zero, it can be compensated by putting a different resistance than channel’s characteristic impedance. For
this case, initial voltage level can be different than its final value and this may cause problems about deciding logic levels. The reflection coefficient on the load side will be zero for the load termination. But if the driver has an output impedance value other than zero, it causes a decrease on the power transfer since there is no control on the impedance for the source side anymore. As a result, double termination is used in most of the high performance serial links to achieve best signal quality because double termination prevents reflections from both ends of the channel.

Termination can be examined also in terms of DC and AC coupled types. In DC coupling, outputs of the transmitter are directly connected to the inputs of the receiver after the channel. Therefore, the common mode of the receiver circuit should be set by transmitter voltage level. In AC coupling, series coupling capacitances are used after the channel. In this connection type, common mode level is determined by the receiver itself. The common mode level should be connected to the signal line via a certain amount of resistance $R_{CM}$ not to decrease the signal level. Because, if the resistance $R_{CM}$ is too small, it creates a voltage divider and drops the signal amplitude.

Finally, passive and active termination topics will be discussed. Passive devices are used in passive termination to create termination impedances. These devices are poly, diffusion or n-well type resistances. In general, poly resistance is the most precise and linear resistance type, also this impedance is usually realized with unsilicided poly. Moreover, MOSFETs can be used as resistors in their linear region with a certain amount of swing limit. Transmission gate structure provides us relatively flat resistance but the threshold voltages change too much with the process variations. Therefore, adjustable resistance structure is needed to obtain a precise active resistance. This adjustment can be done in both analog and digital ways.

2.4 Serializer

Advantages and properties of the serial communication has been explained before. In this part, serializer circuit which is a very essential part of the serial communication system will be discussed. To convert parallel data into serial, serializer circuit is needed; moreover, most of the analog to digital converters are usually designed to give its outputs parallelly. Therefore, serializer is used just before the transmitter and similarly, deserializer circuit is used just after the receiver. Serializer circuit can limit the maximum data rate and this is one of the most important speed limitations of a transmitter system.

2.4.1 Multiplexer Based Serializer

Two distinctive types of serializer circuit topologies are multiplexer based and D flip-flop based serializers. First of all, we will analyze multiplexer based serializer circuit types which are full rate and half rate. In Figure 2.3 full rate multiplexer based serializer structure is shown.
Figure 2.3 Full Rate MUX Based Serializer Structure

2-to-1 multiplexer tree architecture is usually used in MUX based serializer circuits. Full rate architecture uses the clock frequencies clk, clk/2 and clk/4. Therefore, high speed clock signal needs to be generated, routed and divided and this means complexity and the power consumption of the circuit will be increased significantly. Moreover, high speed flip-flop should be designed and used at the end and this element can limit the maximum data rate. On the other hand, the output eye opening does not depend on clock duty cycle since the flip-flop at the end is either rising edge or falling edge triggered. As long as the clock period is constant, the output data will be changed at the right time; therefore, this relaxes the clock duty cycle specification significantly.

Figure 2.4 Half Rate MUX Based Serializer Structure

The half rate multiplexer based serializer structure is shown in Figure 2.4. The same 2-to-1 multiplexer tree architecture is used but there is no flip-flop at the end. Therefore, there is no need for high frequency clock signal. Only frequencies which are used for clock are
clk/2 and clk/4 and this situation reduces complexity and power consumption of the circuit. This architecture employs multiplexer at the end so the high speed flip-flop is eliminated. However, the most important drawback of the system is that there is a clock signal at the select input of the final multiplexer. Since the eye opening of the output is sensitive to duty cycle of the clock signal, if the duty cycle is different from its ideal value which is 50%, the output signal will be effected from this non-ideality. Finally, inputs of the final multiplexer are swapped to prevent possible glitches at the output. Because the zero-input of the multiplexer is connected to the D flip-flop which is triggered by rising edge. Therefore, the input of the multiplexer is already settled before clock goes down to zero. Similar situation applies to the one-input of the multiplexer. Before clock signal goes up, the latch, which changes its output node with the falling edge of the clock, already completes its operation.

2.4.2 D Flip-Flop Based Serializer

Another widely used serializer topology is D flip-flop based serializer. In this architecture, the parallel data is loaded to the outputs of the flip-flop of a shift register. And then, this data is shifted across the shift register in high speed. 4-to-1 D flip-flop based serializer structure is shown in Figure 2.5.

![D Flip-Flop Based Serializer Structure](image)

Figure 2.5 D Flip-Flop Based Serializer Structure

To take the parallel data into the circuit, D flip-flops triggered by parallel clock which is 4 times slower than serial clock are used in our example. After that, load signal becomes active in order to select the parallel data inputs of the multiplexers and set the input nodes of D flip-flops accordingly. Then the selected data is sampled with the rising edge of the serial clock, and then the load signal becomes inactive again. Therefore, the frequency of the load signal is the same as the frequency of the parallel clock and its pulse width is equal to the period of the serial clock signal. After the load signal becomes inactive, the circuit behaves as a shift register. Therefore, the parallel data is transferred to the output node serially.

D flip-flop based serializer has some disadvantages such as flip-flops at the register chain should all be designed as high speed flip-flops since they will be operated at the highest clock frequency on the circuit. On the other hand, multiplexer based serializer circuit can
only be $2^N$-to-1 as we examined before but D flip-flop serializer structure can be designed as N-to-1 while N is an integer.

2.5 Transmitter

Transmitter is one of the key components in the communication systems. Therefore, many different versions of transmitters have been developed with technology in time. In this section, transmitter circuits will be examined in terms of three different aspects which are single ended versus differential, voltage mode versus current mode and pull only versus push-pull respectively.

2.5.1 Single Ended vs. Differential Transmitter

In single ended signaling, only one transmission line is used for transferring the data. If the voltage of the line is higher than the reference value, it is considered as logic 1 and similarly if it is lower than the reference voltage, it is considered as logic 0. Therefore, the line voltage should be compared with the reference voltage in the receiver side. The need of a reference voltage can be considered as a disadvantage of the system. However, only one link is used for transferring one data stream. So, only one pin and one channel is needed for transmitter side. Single ended and differential transmitter examples are shown in Figure 2.6.

![Figure 2.6 Single Ended (a) and Differential (b) Transmitter Examples](image)

For differential signaling, a voltage or current difference is transferred via two lines [7]. Therefore, there is no need for a reference voltage for the receiver; in other words, the signal is self-referenced. The only thing that the receiver should do is to compare voltages at the two lines. Moreover, signal power is double in differential signaling because when one line goes up, the other line goes down and this creates voltage or current difference
which is twice of the amount of voltage or current in single ended signaling. Also, common mode noise or any other non-ideal effect seen in both lines is rejected. Differential signaling is used in most of the high performance communication systems mainly because of its noise immunity property. On the other hand, differential system requires twice the number of pins and lines compared to single ended system and this can be seen as a drawback of this system.

2.5.2 Voltage Mode vs. Current Mode Transmitter

As we discussed before, minimum reflection specification forces us to have double termination which means the output impedance of the driver should be equal to the characteristic impedance of the channel. Since voltage mode transmitters have low output impedances and use Thevenin-equivalent circuit, series termination should be preferred in the driver side. However, deciding the output impedance of the driver is not an easy task, so the resistor that will be put should usually be adjustable. Another topic that we should consider is that the voltage mode driver topology choice depends on output swing specifications. In the Figure 2.7 below, CMOS driver which is a voltage mode driver and is suitable for high output swing is shown. For low swing applications, all-NMOS driver can be used. Finally, it can be mentioned that the voltage mode transmitters have potentially 1/2 to 1/4 of the power consumption of the current mode transmitters [8].

Current mode transmitters can be considered as current sources that change the direction of current according to the data stream. Since the dependence of the current on the drain voltage is almost negligible for current sources, we can claim that the output impedance of current mode drivers is close to infinity. Therefore, in order to have an output impedance equal to the characteristic impedance of the channel, we should use parallel termination. In other words, current mode transmitters use Norton-equivalent circuit which uses parallel termination. Because of that, it is much easier to control output impedance compared to voltage mode transmitters. As an example to the current mode transmitters, the Figure 2.8 from the next section can be given. Similarly, the output swing is easily adjustable with trimming of the current source. So, the same current mode driver can be
used for many different applications or standards by changing the swing. Moreover, current mode transmitters use 2 to 4 times the current of voltage mode transmitters; however, power consumption of the driver is not the only thing that we should consider. Power consumption of pre-driver stage and output impedance adjustment circuit should also be added to the calculation.

2.5.3 Push-Pull vs. Pull-Only Transmitter

The circuits that will be examined under this title are current mode transmitters. Since the current mode drivers are easier to implement and easier to terminate as we have discussed before, they are usually preferred in most of the high speed communication systems. Push-pull and pull-only are the two main types of them and they are slightly different than each other. Push-pull and pull-only current mode driver examples are shown in Figure 2.8.

![Figure 2.8 Push-Pull (a) and Pull-Only (b) Current Mode Transmitters](image)

In push-pull type current mode driver two CMOS inverters are used whose current values are limited by source and sink type two current sources. The circuit has a very good power supply rejection ratio because of two current sources but this can cause headroom problems in low voltage technologies. There are two resistors and they are responsible for providing the output impedance of the driver. Also, using the mid-node of these resistor, the common mode voltage can be changed. Of course common mode voltage cannot be changed in a very wide range because the current sources should be kept in saturation region. As another advantage of the push-pull type driver, output swing can be mentioned. For the same current the output voltage swing is two times higher than pull-only...
type driver. The reason is that CMOS inverter structure uses the same current for both pushing and pulling. This transmitter structure usually known as LVDS driver since it is used in Low-Voltage Differential Signaling (LVDS) standard.

The pull-only current mode transmitter topology is much easier to use in advanced low voltage technologies. Because, it has only one N-type current source and the output voltage of the circuit is higher. As a drawback of this, the circuit has lower power supply rejection ratio compared to the push-pull transmitter. The value of resistors should be equal to the characteristic impedance of the channel. Therefore, the common mode voltage is high and this keeps the current source in saturation region. Output voltage swing is halved compared to the push-pull structure. In other words, to achieve the same swing value, pull-only type driver consumes twice the current. This type of transmitter usually known as current-mode logic (CML) driver.
Chapter 3  Design

3.1  Design Specifications

JESD204B standard supports data rates of the lines for 3 different speed levels. These speed levels are 3.125 Gbps, 6.375 Gbps and 12.5 Gbps respectively. Since our system is planned to have 64-channel ADCs for high speed operation, 12.5 Gbps data rate is aimed to achieve.

This standard includes not only digital blocks to apply the protocol, but also 8-bit / 10-bit encoding which is a transmission code that is used for mapping 8-bit data to 10-bit data for DC balancing [9]. There is a possibility of the random binary data to be all logic-1s or all logic-0s for a long time. In other words, the data that will be sent across a serial link has a possibility to have a long time inactivity or the data can actually be many constant logic values for a significant amount of time. If these situations occur, dc level or common mode value of the line becomes close to either supply voltage or ground and when this happens even if the data inactivity stops, receiver cannot sense the correct data stream until the DC balance of the line is regained. To prevent this bit error problem, 8-bit / 10-bit encoding is usually used in differential data transmissions.

In this encoding, each 8-bit code is represented by a 10-bit code; moreover, the difference between number of logic ones and logic zeros that 10-bit codes have is minimum -2 and maximum +2. That means 8-bit / 10-bit encoding ensures that the long term ratio of logic ones and logic zeros approximates to 50%. For example, 8-bit data 00000000 becomes 1001110100 and 11111111 becomes 1010110001 after this encoding. In other words, for every data, there are enough transitions to have DC balance. These transitions also ease the job of clock data recovery circuit which is in the receiver side. Of course the drawback of this encoding technique is that, the efficiency is 25% decreased since 8-bit data information is sent by 10-bit data stream. Because of that inefficiency, 64-bit / 66-bit encoding which is much more efficient can possibly be used in the future [6].

Because of the fact that JESD204B protocol includes 8-bit / 10-bit encoding, the serializer circuit should be designed 10-to-1. Moreover, as a data rate of the serialized data, 12.5 Gbps is aimed. On the other hand, the transmitter circuit should satisfy not only 12.5 Gbps data rate but also the electrical specifications of the standard given in Table 3.1 [10].
As it is shown in the table, there are both AC and DC compliance modes for transmitter. For AC coupling case, the common mode voltage of the transmitter output can be any value between 0V and 1.8V because a serial capacitance will be used just before the receiver so the receiver circuit will set the common mode. For DC coupling cases, three different common mode specifications for three different termination voltages are defined. Our plan is to use AC coupling so the common mode value can be adjusted to any value between 0V and 1.8V; moreover, this will relax the common mode specification of our transmitter.

### 3.2 Serializer Design

As we have discussed before, JESD204B standard includes 8-bit / 10-bit encoding just like most of the differential standards such as LVDS [11]. This encoding is very useful to obtain the DC balance and to recover the clock and data at the receiver side. Parallel 10-

---

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>UI</td>
<td>Unit Interval</td>
<td>Baud Rate=1/UI</td>
<td>80</td>
<td>156.9</td>
<td>ps</td>
</tr>
<tr>
<td>T_Vcm</td>
<td>Common Mode</td>
<td>AC coupling (Z_{tt} \geq 1k\Omega)</td>
<td>0</td>
<td>1.8</td>
<td>V</td>
</tr>
<tr>
<td>T_Vcm</td>
<td>Common Mode</td>
<td>DC coupling (Z_{tt} \leq 30\Omega) (V_{tt}=1.2V)</td>
<td>735</td>
<td>1135</td>
<td>mV</td>
</tr>
<tr>
<td>T_Vcm</td>
<td>Common Mode</td>
<td>DC coupling (Z_{tt} \leq 30\Omega) (V_{tt}=1.0V)</td>
<td>550</td>
<td>1060</td>
<td>mV</td>
</tr>
<tr>
<td>T_Vcm</td>
<td>Common Mode</td>
<td>DC coupling (Z_{tt} \leq 30\Omega) (V_{tt}=0.8V)</td>
<td>490</td>
<td>850</td>
<td>mV</td>
</tr>
<tr>
<td>Vdiff</td>
<td>Transmitter Differential Voltage</td>
<td>Into floating 100(\Omega) load</td>
<td>360</td>
<td>770</td>
<td>mVppd</td>
</tr>
<tr>
<td>Idshort</td>
<td>Short Circuit Current</td>
<td>Terminals shorted to each other or ground</td>
<td>-100</td>
<td>+100</td>
<td>mA</td>
</tr>
<tr>
<td>Zddiff</td>
<td>Differential Impedance</td>
<td>At DC</td>
<td>80</td>
<td>120</td>
<td>(\Omega)</td>
</tr>
<tr>
<td>RLldiff</td>
<td>Differential Output Return Loss</td>
<td>From 100MHz to 0.75*Baud Rate</td>
<td>8</td>
<td></td>
<td>dB</td>
</tr>
</tbody>
</table>

Table 3.1 JESD204B Standard Transmitter Electrical Specifications
bit data stream whose frequency is 1.25 GHz is the input, 12.5 Gbps data rate single line is the output of the serializer circuit.

Because of this encoding technique, 10-to-1 D flip-flop based serializer architecture that is examined before is used since the multiplexer based serializer topology is restricted only to be $2^N$-to-1 while N is an integer. Designed serializer circuit is shown in Figure 3.1.

![Figure 3.1 Designed Serializer Circuit](image)

The aim of the circuit is to load the parallel data to the internal nodes of shift register and take this data to the output node serially with a fast clock signal. The first design consideration is to use half-rate structure because achieving 12.5 Gbps data rate with full-rate structure needs all the circuit elements to operate at 12.5 GHz which is very difficult and power hungry. Therefore, two flip-flop lines are designed and the upper one is for even bits, lower one is for odd bits. Every flip-flop has a multiplexer which is responsible for driving the input node of flip-flops when the parallel data is loaded.

There are two different clock signals in the circuit. The first clock signal is parallel clock which has 1.25 GHz frequency. This clock is responsible for bringing 10-bit parallel data stream in every period. The second clock signal is serial clock which is responsible for shifting the loaded data and its frequency is 6.25 GHz. Since the half-rate architecture is used, 12.5 GHz clock is not needed and the last multiplexer selects even bits and odd bits one by one. Moreover, the load signal should be generated to load the parallel data into the inputs of the flip-flops and these data should be sampled by flip-flops with fast serial clock. To do so, load signal should be activated once in every parallel clock period and becomes inactive again after one serial clock period. The circuit generating the load signal is shown in Figure 3.2.
What is done in the design of load generation circuit is sampling of the parallel clock with a flip-flop which is triggered by the serial clock. Also, another flip-flop is added in series to the first sampling flip-flop to have two different phases of parallel clock. This phase difference is one serial clock period. After that, if the OR operation is performed with the second sampled clock and the inverse of the first sampled clock, the load signal is obtained at the output. Since the load signal becomes active with logic zero in this circuit, the output of OR gate can directly be connected to the select inputs of the multiplexers. On the other hand, parallel clock and serial clock are generated by ideal voltage sources synchronously in the testbench. Because the plan for whole system is the generation of both of the clocks by the same phase locked loop circuit so that they become synchronized. By this means, it will be possible to sample parallel clock with the serial clock and generate the load signal.

However, in this case, synchronization of rising or falling edges of the clock signals can create metastability problem. To prevent metastability danger, in addition to the synchronization of these two clock signals, there should be enough delay between each other. If this is not possible because of the restrictions of PLL circuit, another solution can be carefully delaying one of the clock signals in order to have similar waveforms.
Since the half-rate architecture is used, the maximum clock frequency is 6.25GHz in the circuit. But it has an important disadvantage about the dependence of output eye opening to clock duty cycle. There is a 6.25 GHz clock signal at the select input of the final multiplexer. The more duty cycle of this clock deviates from 50%, the smaller the eye opening becomes at the output. To fix this dependence, another flip-flop can be used after the multiplexer but that final flip-flop needs 12.5 GHz clock so, this solution is not very efficient. Therefore, instead of high-speed flip-flop solution, duty cycle of the 6.25 GHz clock should carefully be delivered. Moreover, the final multiplexer and the previous flip-flops use the same high-speed clock. Because of the clock to Q delay of the flip-flops when the clock goes high, the inputs of the multiplexer will not be settled yet. So at the final output there will be some undesired glitches. To prevent these glitches, a falling edge flip-flop is added to the 1-input of the multiplexer.

To show the data rate which is 6.25 Gbps easily, all the even bits are set to logic 0 and all the odd bits are set to logic 1 in Figure 3.4. Just after the deactivation of the load signal, bit 9, bit 8 ..., bit 0 can be seen at the output respectively.

![Figure 3.4 Output Waveform of the Serializer for the Input = 1010101010](image)

First of all, flip-flops and multiplexers are tested from standard cell libraries to understand if they are fast enough for this data rate. After that, these gates are placed manually to minimize the routings and to provide good matching between two 5-bits line. Also a lot of MOS capacitances are used between supply and ground for minimizing voltage drops. The circuit is tested in every process corner and it is assured that there is no bit error at the output. The layout of the serializer is shown in Figure 3.5. Its layout dimensions are 20.3 µm to 16.4 µm.
3.3 Transmitter and Its Building Blocks

To explain the design of the transmitter system, first the core part of the transmitter, secondly the current sources, then the operational transconductance amplifier and finally the common mode feedback system will be examined.

3.3.1 Transmitter Design

As it is explained before, current mode transmitters have a lot of advantages; for example, they are easy to implement, easy to adjust voltage swing and output impedance of a driver for parallel termination. Therefore, pull-only current mode transmitter and push-pull current mode transmitter circuits are designed and compared. With a good design of current mirrors and transmitter itself, keeping current sources in saturation region was not an issue. On the other hand, push-pull transmitter consumes half the power of pull-only transmitter. When all this reasons are combined, designing push-pull current mode transmitter seems reasonable. In Figure 3.6, transmitter topology which is used in this design is shown.

Figure 3.5 The Layout of the Serializer
The inverters connected to the data inputs of the transmitter should be designed carefully. PMOS and NMOS current sources must be kept in saturation region, so the W/L ratios of the inverter transistors should be big enough to keep them in saturation. As a result, drain voltage of NMOS current source is around 312mV and drain voltage of PMOS current source is around 672mV and these values are more than enough for $V_{DS}$ voltages of the current sources.

In order to have a balanced inverter, the transconductances of PMOS and NMOS transistors should be equal. Thus, the circuit responds symmetrically for both rising and falling edges. Since FD-SOI technology is used, threshold voltages can be adjusted by changing the bulk voltages. For both NMOS and PMOS, the bulk voltage can be any value between $V_{DD}$ and GND and the table below shows the threshold values of transistors for end values. The most balanced threshold values are achieved with connecting the bulk of PMOS and NMOS transistors to GND.

<table>
<thead>
<tr>
<th></th>
<th>$V_{bulk} = GND$</th>
<th>$V_{bulk} = VDD$</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>NMOS Vth</strong></td>
<td>0.387 V</td>
<td>0.296 V</td>
</tr>
<tr>
<td><strong>PMOS Vth</strong></td>
<td>0.386 V</td>
<td>0.464 V</td>
</tr>
</tbody>
</table>

Table 3.2 Threshold Values for Different Bulk Voltages

Another part of the transmitter circuit is single ended to differential converter. The serializer output is single ended and it needs to be converted into differential signals before the driver circuit. Therefore, for one input, the inverter chain is used and for the other input, a transmission gate which is always ON is used for the first inverter of the chain. At the
end, two different phases of the digital signal are obtained. Depending on the performance of the circuit in corner simulations, cross coupled inverters can be used in order to be sure that these two phases will exactly be the opposite of each other’s.

The layout of the transmitter is shown in Figure 3.7. NMOS and PMOS current sources are not included in this layout; however, inverters and resistors are included. High precision poly resistors are used in order to have exactly 50 Ω. The most challenging design consideration of the layout was the electromigration rules. The transistors and wires conduct 2.5 mA and thick wires with top metals and a lot of vias are used in order not to violate electromigration rules. The dimensions are 23.1µm to 23.5µm.

![Figure 3.7 The Layout of the Transmitter](image)

### 3.3.2 Current Source Design

The challenging part in the design of push-pull current mode transmitter which is also known as LVDS driver is that it is difficult to keep both NMOS and PMOS current sources in saturation region for low voltage technologies. In order to avoid any saturation problem, current sources should carefully be designed.

To do so, 10uA unit current is selected for a unit transistor. The drain voltage of the current source is limited by 180mV in the testbench. This means the current sources are designed to be in saturation region for every corner with 180mV drain voltage. Normally,
nominal $V_{DS}$ voltage of the current sources is 312mV when they are connected to the transmitter. This ensures that the current sources cannot have any saturation problem in the transmitter circuit. This unit current source and its multiples are planned to be used in transmitter and OTA circuits. Therefore, the mirroring performance is also an important parameter. So the long channel devices are used in order to achieve better mirroring performance. The corner simulation results are shown below. Nominal supply voltage is 1V and 10% supply voltage deviation is considered in those simulations. In addition to the process corners such as slow and fast, the temperature is swept between -40°C and 120 °C.

<table>
<thead>
<tr>
<th>Parameter (NMOS)</th>
<th>Nominal</th>
<th>Minimum</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{drain}$</td>
<td>9.804 uA</td>
<td>9.755 uA</td>
<td>9.836 uA</td>
</tr>
<tr>
<td>$V_{dsat}$</td>
<td>157.8 mV</td>
<td>135.8 mV</td>
<td>173.5 mV</td>
</tr>
<tr>
<td>$V_{ov}$</td>
<td>22.25 mV</td>
<td>6.45 mV</td>
<td>44.23 mV</td>
</tr>
<tr>
<td>$Gm$</td>
<td>143.8 uS</td>
<td>125.4 uS</td>
<td>176.1 uS</td>
</tr>
</tbody>
</table>

Table 3.3 Corner Simulation Results of NMOS Current Source

<table>
<thead>
<tr>
<th>Parameter (PMOS)</th>
<th>Nominal</th>
<th>Minimum</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{drain}$</td>
<td>9.903 uA</td>
<td>9.864 uA</td>
<td>9.919 uA</td>
</tr>
<tr>
<td>$V_{dsat}$</td>
<td>-157.4 mV</td>
<td>-173.2 mV</td>
<td>-131.2 mV</td>
</tr>
<tr>
<td>$V_{ov}$</td>
<td>22.6 mV</td>
<td>6.84 mV</td>
<td>48.77 mV</td>
</tr>
<tr>
<td>$Gm$</td>
<td>143 uS</td>
<td>124.5 uS</td>
<td>183.4 uS</td>
</tr>
</tbody>
</table>

Table 3.4 Corner Simulation Results of PMOS Current Source

3.3.3 Operational Transconductance Amplifier Design

As it is shown in the schematic before, operational transconductance amplifier (OTA) is needed for common mode feedback of the transmitter. In the design of OTA, matching of current sources and differential pair transistors are very important to reduce the offset voltage. Therefore, the same unit current sources are used in also OTA. To be able to have a decent gain with 1V supply voltage, symmetrical OTA structure is used in the design. [12]. This circuit also provides lower offset and better CMRR because differential pair transistors have exactly the same load which provides better symmetry.
This design has only one high impedance node which is the output node. Impedances of all the other nodes are around $1/gm$ so this is a single stage OTA. The load of the differential pair is two current mirrors that provide a certain amount of gain. As the current mirror ratio increases, the gain increases but also the parasitic capacitances at the gate nodes of the current mirrors increases and this brings the non-dominant pole to the lower frequencies. Therefore, there is an optimum value for the current mirror ratio which depends on the load capacitance and it is selected as 4 in this design.

For the differential pair transistors, the most important design parameters were the biasing conditions of the tail current mirror and the offset voltage. W/L ratio should be big enough to keep the tail current source in saturation and W*L product should be big enough to decrease the offset to the acceptable limit. Gain and phase waveforms of the OTA is shown in Figure 3.9. There is 2.5 pF load capacitance at the output.
In order to be sure that OTA operates properly in every process, supply voltage and temperature corner, corner simulations have been done. The results are shown in Table 3.5.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Nominal</th>
<th>Minimum</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Gain</td>
<td>56.99 dB</td>
<td>54.51 dB</td>
<td>60.51 dB</td>
</tr>
<tr>
<td>UGBW</td>
<td>61.62 MHz</td>
<td>52.31 MHz</td>
<td>82.93 MHz</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>54.56 °</td>
<td>50.81 °</td>
<td>56.59 °</td>
</tr>
</tbody>
</table>

Table 3.5 Corner Simulation Results of the OTA
It is desired to determine the common mode voltage with a certain precision. In this design the precision limit is decided as ±2mV. In other words, in order to set the common mode voltage that is suitable to the specifications, the offset voltage of the OTA should be less than 2mV. Differential pair transistors are the most critical elements for the offset and the gate areas of the transistors are designed to be big enough to fulfill this specification. The histogram of the offset voltage is shown in Figure 3.10.

The 200 sample Monte Carlo simulation results showed that the standard deviation of the offset value is 1.284mV while minimum value is -3.728mV and the maximum value is 4.48mV. Moreover, 88% of the samples were in ±2mV range which seems acceptable for our specifications.

Finally, the layout of the OTA is shown below. To get rid of the stress caused by field oxide at the active region, 4 finger dummy transistors are used at the both sides of the differential pair. Also interdigitizing technique is used for all of the transistors in OTA. The final layout dimensions are 17.5µm to 14.5 µm.

3.3.4 Common Mode Feedback

The OTA that is explained before is used in common mode feedback (CMFB) system. If the voltage level at the middle point of the outputs of the transmitter increases, the positive input voltage of the OTA becomes higher than its negative input voltage. OTA output voltage increases and current of the tail NMOS increases. Since the constant current is pushed by the PMOS current source, current pulled by NMOS becomes higher and volt-

![Figure 3.11 The Layout of the OTA](image-url)
ages of all of the internal nodes of transmitter decreases including the middle point of the outputs. This is how the negative feedback system works.

In order to assure that this feedback system is stable, 2.5pF load capacitance at the output node of the OTA is not enough. Because common mode feedback loop has another gain stage which is the NMOS current source that behaves as a common source amplifier. Therefore, another high impedance node is created at the drain of the NMOS which is at the tail of the transmitter and the system becomes two stage amplifier. To split these two poles, capacitance at the output of the OTA is increased to 3.7pF and is used as Miller capacitance. In other words, capacitance is connected between the output of OTA and drain of tail NMOS. Thus, using relatively small capacitance, the effect of big capacitance can be achieved using Miller effect. The gain and phase plots of the common mode feedback loop is shown Figure 3.12.

![Gain Phase Plot of the CMFB](image)

Figure 3.12 Gain Phase Plot of the CMFB

With 3.7pF Miller capacitance, DC gain of the common mode feedback is 55.88dB and phase margin is 82.7°. In order to decrease the response time, phase margin can be decreased around 60° using smaller capacitance.

3.4 Modeling of PCB Trace

The aim of this project is to design a transmitter circuit which is responsible for delivering the ADC outputs to the receiver which is also JESD204B compliant. In addition to the chip parasitics, there will be a printed circuit board transmission line at the output of the transmitter. In order to model this PCB trace, microstrip line element is used in ADS environment. Microstrip line is a kind of transmission line that is manufactured using PCB technology. It consists of three different layers which are conductor, dielectric substrate and ground plane. The cross section is shown below in Figure 3.13.
In order to model the microstrip line the parameters which are used in ADS environment simulations are listed in Table 3.6.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>Substrate Thickness</td>
<td>0.254 mm</td>
</tr>
<tr>
<td>Er</td>
<td>Relative Dielectric Constant</td>
<td>4.5</td>
</tr>
<tr>
<td>Cond</td>
<td>Conductivity</td>
<td>5.8E+7 S/m</td>
</tr>
<tr>
<td>T</td>
<td>Conductor Thickness</td>
<td>35 µm</td>
</tr>
<tr>
<td>TanD</td>
<td>Dielectric Loss Tangent</td>
<td>0.02</td>
</tr>
<tr>
<td>Z0</td>
<td>Characteristic Impedance</td>
<td>50 Ω</td>
</tr>
<tr>
<td>E_Eff</td>
<td>Electrical Length</td>
<td>2154 °</td>
</tr>
<tr>
<td>L</td>
<td>Physical Length</td>
<td>100 mm</td>
</tr>
<tr>
<td>W</td>
<td>Physical Width</td>
<td>0.456 mm</td>
</tr>
</tbody>
</table>

Table 3.6 Parameters of 100 mm Line for FR-4

LineCalc tool is used for modeling the microstrip line properly. Dielectric substrate is considered as FR-4 material and the parameters are given accordingly. The characteristic impedance of the line is arranged to 50 Ω with the given width of the conductor. In fact, two different PCB lines that are 100 mm and 40 mm are modeled to see the effect of the channel length. Electrical length is 861.6 ° for 40 mm line while it is 2154 ° for 100 mm line. As a result, the loss along the channel will be different for different lengths. This difference will be shown in s-parameter simulations of the channels.

After modeling the trace, s-parameters are extracted from ADS in order to be used in Cadence environment. S-parameter simulations are run, s11 and s21 characteristics of 40 mm and 100 mm length channels which are properly terminated are shown.
Since the FR-4 parameters have a loss tangent value which is different than zero, the line model has a loss and this loss means decrease in signal power especially in high frequencies. If we compare the two lines with different lengths, s21 of the 40 mm line is always greater than -3dB up to 20 GHz while the s21 of 100 mm line is approximately -7dB at 20GHz. Decrease in signal power can be critical if the circuit operates at the edge of the voltage swing specifications of the standard. In terms of s11, there is no danger of reflection because s11 values are always below -35dB. Of course it should be kept in mind that the lines are terminated ideally. In a real circuit, termination should not be expected to be perfect.

Moreover, to model the parasitic elements of the lines which are placed close to each other, microstrip coupled line instance is used. Thanks to this element, parasitics such as mutual inductance and coupling capacitances can be modeled. The cross section of a microstrip coupled line is shown in Figure 3.16.
In this microstrip line model, the same dielectric substrate and conductive line parameters are used. The spacing between the lines is chosen as the same with the line width which is 0.456 mm. With the given parameters, even-mode impedance is 53.17 ohm while odd-mode impedance is 45.07 ohm.

3.5 Top Level Simulation Results

The PCB trace and its termination resistance is not the only load that the transmitter should drive. There are also capacitances that comes from ESD diode, IO pad, and package connection. Moreover, bondwire and its connection create inductance and resistance. In order to model all these elements basically, 10 Ω resistance and 1nH inductance have been included in series branch to model the bondwire and connection. Also, 100 fF capacitance has been put in parallel branch to model the package parasitic. The other capacitances that come from ESD diode and pads are extracted thanks to parasitic extraction tool which estimates the values more realistically. Finally, there is 100 Ω differential resistance after PCB trace to model the input impedance of the receiver.

As it is mentioned in design specifications part, one of the electrical specifications of the transmitter is that differential output return loss should be at least 8 dB at 0.75*Baud Rate. In other words, if we look at the transmitter from outside of the chip, s11 should be maximum -8 dB at 9.375 GHz. S11 of the transmitter is shown in Figure 3.17. Bondwire and package parasitics are included in this simulation. Because of the bondwire inductance in series path, differential impedance and s11 of the transmitter increases. The result is -8.182dB which is very close to the -8dB limit.
For data rate results, serializer and transmitter are tested together. Thanks to random bit stream instance, random data streams are given to the serializer in order to test the circuits realistically. To measure the quality of the signal at the input of the receiver, eye diagram method is used. In eye diagram tool, simulator basically divides the transient response into one period intervals then plots them on top of each other. By this way, transition performances of every input combination can be seen. The figures below show the eye diagram of the differential signal between the terminals of 100 Ω resistance which comes after PCB trace. Eye diagram opening is wider for the 40mm line compared to 100mm. Since the decrease on s21 at high frequencies are higher for the 100mm line, transitions become slower.

Finally, the average current consumption of the serializer is 522 µA while it is 4.026 mA for the transmitter. This measurement is done with a testbench setup which has frequent transitions.
Figure 3.18 Eye Diagram for 40mm Line

Figure 3.19 Eye Diagram for 100mm Line
As it is mentioned before, this transmitter circuit is planned to be used in 64-channel high-speed ADC system. To test the multi-channel performance of the circuit, simple 4-channel testbench is designed. Mutual inductances which have 0.2 coupling coefficient are placed between the bondwire inductances of different channels. Also 100fF coupling capacitances are placed before and after the PCB line in between different channels. In this way, a simple model of the close bondwire and PCB lines is obtained and simulated. Moreover, to model the clock skew between channels, 0ps 40ps 80ps and 120ps delays are given for these four lines respectively. Differential output voltages for four different channels at the input impedance of the receiver is shown in Figure 3.20.

![Figure 3.20 Eye Diagram of Four Different Channels](image)

As a result, it can be stated that the inner channels have worse eye openings than the outer channels. This is mainly because of the fact that, both differential lines of the inner channels are affected by their neighbor channels while only one line of the outer channels is affected by their neighbor channels. These eye openings may be good enough but if better performance is needed or worse parasitics occur, an easy solution can be placing VDD and/or GND pins and lines in between the data lines. In this way, coupling coefficient of the mutual inductance and the values of coupling capacitances between the data lines can be decreased.
Chapter 4  Tape-Out Work

The transmitter part of the system has been taped out to see if the circuit functions properly. The serializer circuit was not ready on the deadline date; therefore, this part is not included. The layout of the work which is sent for manufacturing is given in Figure 4.1.

Figure 4.1 The Layout of the Tape-Out Work

This tape-out will be really useful to have an idea about the parasitic elements that come from electrostatic discharge (ESD) diodes and pads. Because, these elements are sources that limit the performance of a transmitter. This circuit is designed to transfer the ADC
data to the FPGA but the connections from JESD204B protocol circuit to ADCs and transmitter has not been completed yet. So, the aim of this tape-out is to see if the transmitter can reach the target data rate which is 12.5 Gbps. In order to test it, 6.25 GHz clock signal produced by the PLL circuit which is in the same chip is given to the data input of the transmitter. 6.25 GHz clock also means 12.5 Gbps data that constantly changes its bits. Moreover, another input is also added to the circuit in case of a problem with high-speed clock. This input is connected to a pad and low-speed clock signal will be given from outside of the chip.

Another advantage of this tape-out is about the electromigration rules of the process. The core of the transmitter circuit consumes constant 2.5 mA current and its layout has been drawn to fulfill the electromigration rules. Also, the rest of the circuit carries some high frequency signals which leads to significant increase in peak current that is pulled from the source. Since the peak and average current consumption have both been very high, these rules were the most challenging part of the layout. Checking the functionality of the circuit will also be very helpful for this issue.
Chapter 5  Conclusion

5.1 Achieved Results

The serializer and transmitter circuits have been designed and their layouts have been drawn. After parasitic extraction, the circuit does fulfill the specifications of JESD204B standard. Serializer circuit is able to take 10-bit parallel data at 1.25 Gbps as an input and transforms these bits into 12.5 Gbps serial output. Parasitics of the integrated circuit, bondwire, package and PCB transmission line have been modeled. Between the terminals of 100Ω resistance which comes after PCB line, the eye opening of the data stream is very wide. After merging with the JESD204B protocol circuit, it will be ready to transfer the ADC outputs to another integrated circuits which has receiver that is compliant with the same standard.

5.2 Future Development

First of all, sub-blocks of the circuits have been tested in process corners but the extracted view of the circuit has only been tested in typical corner. It can be simulated in every corner to find out if there is any problem. Moreover, the bias current of the transmitter is constant which causes constant voltage swing. Therefore, current adjustment circuit can be added to the current source to trim the voltage swing. Single ended to differential converter may cause eye opening problems in process corners. If this occurs, cross coupled inverters can be used to be sure about the quality of the differential signals.

Also pull-only current mode transmitter topology can be designed in order to try DC coupling since that driver circuit is more suitable for JESD204B common mode specifications. Furthermore, behavior of a real PCB trace can be compared with the one that is modeled in ADS environment by doing measurements with the transmitter which has been taped-out. Finally, the data rate can be tested to go beyond 12.5 Gbps because even if the JESD204B standard supports up to this speed, FPGAs with faster receivers can be found today.
References


