Ultra-Low-Power and Widely Tunable PLL

Master Thesis

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Abstract

Cutting edge technology applications continuously seek for alternative circuit design methodologies offering low power consumption. Driven by this motivation, several techniques such as ‘Sub-threshold CMOS’, ‘Source Coupled Logic (SCL)’ and ‘Sub-threshold SCL (STSCL)’, which is the combination of ‘Sub-threshold CMOS’ and SCL, have been introduced. STSCL consumes low power and enables implementation of widely adjustable circuits. However, these advantages bring forth the need for wide tuning range clock generators. To accomplish this need, widely tunable and power scalable phase-lock-loop (PLL) design is targeted.

This report presents an adaptive-bandwidth self-biased approach for achieving such a PLL. The determination of design parameters is realized through a system level analysis. And, the PLL is implemented in a conventional 90nm CMOS technology. The design process was mixed-signal, and STSCL has been the integral part for digital PLL blocks such as ring oscillators and frequency dividers. The interface between STSCL and CMOS logic is composed carefully. Moreover, stability requirements are foreseen at each step. Based on the proposed topology, power consumption and loop dynamics could be scaled with respect to the operation condition. The measurements show that the PLL achieves an output frequency range of 32 KHz – 3.2 MHz with a bias current range of 1.35 nA- 142.7 nA. At 32 MHz oscillation frequency, the PLL consumes 8.2µW, while it consumes 2.8µW at 32 KHz.

**Key Words:** Subthreshold Source Coupled Logic (STSCL), clock generation, phase-locked loop (PLL), adaptive-bandwidth, self-biased, ultra-low-power circuits.
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1. Introduction

1.1. Motivation

From the invention of the integrated circuit (IC), year 1958, to date, the trend in IC design has been to scale down the minimum feature size. Today, deep-submicron technologies are extensively used for the design of ICs. According to 2009 ‘International Technology Roadmap for Semiconductors’ (ITRS), in the next 15 years, technology scaling will continue.

<table>
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<tr>
<td>Feature size(nm)</td>
</tr>
<tr>
<td>Vdd (V)</td>
</tr>
<tr>
<td>Power (W)(heat sink)</td>
</tr>
<tr>
<td>2009</td>
</tr>
<tr>
<td>38</td>
</tr>
<tr>
<td>1</td>
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The predictions of Table 1-1 suggest that supply voltage scaling and power consumption will be the design challenges of the upcoming years.

Supply voltage value is a critical parameter for power consumption. Scaling down its value would scale down the power consumption. However, if the technology roadmap observations for years 2009 and 2012 are compared, it is observed that despite the decrease in the value of power supply, the power consumption has increased. Therefore, new design approaches are demanded for low power ICs. Sub-threshold source-coupled logic (STSCL) is a design technique that is offered to fulfill this demand. In STSCL design, the transistors are biased in sub-threshold regime; and this property offers an advantage of very low power consumption [1].

Another important feature of STSCL to be investigated is circuit operation over a very wide frequency range without any need to scale the sizes of devices [1]. But, to adjust the operating frequency of circuits designed with this logic, widely tunable clock generators are needed.

Most of the time, clock generation is realized by units called phase-locked loop (PLL). This unit has found broad usage in many applications of electronics and communications [2]. Examples of such applications are frequency multiplication and synthesis, signal recovery circuits and clock distribution in digital systems.

Wide tuning range PLL is a class of PLLs that is able to provide scalable output frequency by adjusting the loop dynamics proportionally with the operation condition [3, 4]. Therefore; in order to completely benefit from wide frequency range operation property of STSCL, wide tuning range PLLs should be used side by side with circuits implemented by this logic. In such a case, wide tuning range PLLs will adjust the operating conditions of low power
STSCL circuits; hence, they need to be low power circuits, as well. In addition, their power consumption should scale with operating frequency. An easy way to obtain a PLL with these adjustable characteristics is to design the PLL with an STSCL topology.

In literature, several techniques for designing PLLs with limited tuning range and wide tuning range have been studied [2-6]. However, design of wide tuning range PLLs with an STSCL topology is still an open research subject. In this project, the aim is to implement a widely tunable and power scalable PLL with an STSCL topology in a conventional 90nm CMOS technology.

1.2. Thesis Organization

In Chapter 2, the fundamental characteristics and building blocks of PLLs and charge-pump PLLs (CPPL) are presented along with stability requirements and brief noise analysis. Chapter 3 shortly explains the wide tuning range PLL design procedure and lists the related issues. Chapter 4 first presents the proposed PLL topology. Then, it introduces a background for STSCL design. Afterwards, the whole steps taken for the system level design and transistor level design are discussed. Performance measurements will also be summarized under this heading. Chapter 5 demonstrates the achievements of presented study, explains the future work and provides the concluding remarks.
2. Phase-Locked Loop Fundamentals

2.1. Basic PLL Topology

A phase-locked loop (PLL) is a feedback system that generates a well-timed periodic signal whose phase is aligned with the phase of a reference signal. As shown in Figure 2-1, it consists of three basic blocks: phase detector (PD), low-pass filter (LPF) and an oscillator.

The PD compares the phase of the reference signal and the phase of the output signal. It produces an error signal which is proportional to the phase difference of its two input signals. The output of PD is filtered to suppress the high frequency components and then is applied to the oscillator as a controlling signal (voltage or current). The output frequency of the oscillator is adjusted by this controlling signal in a way to decrease the phase difference. The loop is locked, when the phase difference does not change with time. If the loop is locked, the phase difference is constant and preferably small [5]. Also, in this condition, the frequency of the PLL output signal is the same as that of the reference signal. A frequency divider can be added to the feedback path as used in Figure 2-1. The functionality of this new block is to divide the oscillator frequency by a factor $N$. In this new configuration, the output frequency of the oscillator will be equal to $N$ times the reference frequency.
2.2. Charge-Pump PLL and PLL Building Blocks

Figure 2-2 represents the block diagram of a charge pump PLL. This type of PLL consists of five sub-blocks: phase/frequency detector (PFD), charge pump, loop filter, oscillator and frequency divider. The functionalities of these blocks are described below.

![Block Diagram of Charge-Pump PLL](image)

**Figure 2-2: Charge-pump PLL (CPLL) topology**

### 2.2.1. Oscillator

An oscillator produces periodic signals such that the circuit has no input while maintaining the output definitely [5]. Figure 2-3 shows a CMOS ring oscillator which is an oscillator type consisting of a number of delay stages in a loop. Since, in this project, a ring oscillator will be used; its properties will be explained below. Information about other types of oscillators can be found in [5, 6].

![Ring Oscillator](image)

**Figure 2-3: Three-stage ring oscillator**

Figure 2-3 is a three-stage ring oscillator circuit. It consists of identical inverters. The only DC operating point, at which the input and output voltages of all inverters are equal to the
logic threshold $V_{th}$, is inherently unstable [7]. Any disturbance in one of the input or output voltages would make the circuit astable.

By assuming equal output load capacitances at all nodes and considering that the inverters are identical, the oscillation period $T$ of the ring oscillator can be calculated in terms of the average propagation delay $\tau_P$ [7], as follows:

$$ T = \tau_{PH1} + \tau_{PLH1} + \tau_{PHL2} + \tau_{PLH2} + \tau_{PHL3} + \tau_{PLH3} $$

$$ = 2 \tau_P + 2 \tau_P + 2 \tau_P = 6 \tau_P $$

If the relationship is generalized for any odd number $n$, the oscillation frequency is obtained by

$$ f = \frac{1}{T} = \frac{1}{2n \tau_P} $$

The frequency of the ring oscillator can be adjusted by controlling $\tau_P$. And this average delay value can be tuned by changing the supply (voltage or current) of inverters. If the control parameter is a voltage value then the oscillator is called voltage-controlled oscillator (VCO). On the other hand, if the control parameter is a current value, then the type is current-controlled oscillator (CCO). The gain of the oscillator is defined as the slope of output frequency versus control signal curve. It represents the sensitivity of the oscillator. The symbol of the gain is denoted as $K_{VCO}$ or $K_{CCO}$ and is given by

$$ K_{VCO} = \frac{\partial w_{out}}{\partial V_{cont}} \quad K_{CCO} = \frac{\partial w_{out}}{\partial I_{cont}} $$

Lastly, it should be noted that with CMOS inverters, only cascade of odd number of inverters will act as an oscillator. However, with STSCL inverters cascade of both odd and even number of inverters will display oscillatory behavior. This property will be analyzed in section 4.3.5.5.

### 2.2.2. Frequency Divider

A frequency divider is a circuit that divides the frequency of its input signal by a factor $N$, where $N$ is an integer. When used in a PLL, this block divides the oscillator output frequency. It is also possible to place a frequency divider to divide the input reference frequency. A simple example of a frequency divider is a divide-by-two circuit as shown in Figure 2-4.
The circuit consists of one D flipflop with its inverted output connected to its input D. Consider the initial value of Q as logic high and the flipflop as rising-edge triggered. When a rising edge of clock arrives, Q is set to logic low. The output will stay in this condition until the next rising edge. Then, it will be set to logic high again. Hence, when an input signal with frequency $f$ is applied from CLK input, the frequency of output $Q$ will be $f/2$.

In other PLL systems, like fractional $N$ systems, two different division ratios are needed. Therefore, both divide-by-N and divide-by-(N+1) dividers are used. And with a modulus controller, $N$ is toggled between numbers [6]. In this project, the frequency divider will be constructed using only divide-by-two circuits. Further information about the other type of frequency divider can be found in [6].

### 2.2.3. Phase/Frequency Detector

A phase/frequency detector can detect both phase and frequency differences. It provides an error signal that is proportional to the phase and frequency difference between the two inputs. Conceptual operation of a PFD can be indicated by the two cases [5] in Figure 2-5.
In Figure 2-5 (a), the two inputs have the same frequency, but the rising edges of A arrive earlier. For this case, Q_A generates pulses whose width is a function of the phase error $\theta_A - \theta_B$ and the output Q_B remains silent. In Figure 2-5 (b), signal A has a higher frequency than other input. Q_A produces pulses to correct the frequency error while Q_B stays at zero. The PFD is designed as a symmetrical circuit. Therefore, if the rising edges of B arrive earlier or B has a higher frequency than signal A, then the output Q_B produces pulses and Q_A does not.

The operation of PFD circuit can also be represented by a state machine with three states as illustrated in Figure 2-6 (a). In a PLL, the inputs of the PFD are the reference signal (ref) and the divided output (div). This machine can respond to either rising or falling edges of the inputs.

![State machine diagram](image)

![Schematic of PFD](image)

**Figure 2-6: State machine and schematic of PFD**

Figure 2-6 (b) demonstrates an implementation of PFD with two flip-flops and one AND gate. The previously mentioned output signals Q_A and Q_B refer to Up and Down signals, respectively. The reference signal and the divided output signal are given to the clocks of the flip-flops. Assume that both Up and Down signals are logic low. When a transition occurs in reference signal, Up will rise to logic high value. While the circuit is in this state, a transition in divided output signal changes the Down value to logic high. With both Up and Down being
equal to logic high, the output of the AND gate becomes logic high and resets both flip-flops. This operation can also be followed from the state machine of Figure 2-6 (a).

2.2.4. Charge Pump
The charge pump circuit (CPC) consists of two switchable current sources. The circuit model is shown in Figure 2-7.

![Figure 2-7: Charge pump circuit (CPC)](image)

The switches are driven by the Up and Down signals of the PFD. When Up signal is high, the CPC supplies current $I_{UP}$ and injects charge into a capacitor that would be placed at the output of the charge pump. When Down signal is high, the CPC supplies $-I_{DN}$, in other words it discharges the capacitor. The output of the CPC drives the loop filter.

2.2.5. Loop Filter
In a CPLL, the loop filter (LF) generates the controlling signal of the oscillator. A simple loop filter can be designed with a single capacitor as depicted in Figure 2-7. As will be explained later in section 2.4, the oscillator creates a pole at the origin. The capacitor of the LF also introduces a pole at the origin. The two poles at the origin make the loop unstable. The remedy to solve the instability is to introduce a zero in the loop by adding a resistor in series with the capacitor. Furthermore, in a real PLL implementation, the output of charge pump is not a pure DC signal. It also contains AC components which cause ripples on the controlling signal [5]. In order to reduce these ripples another capacitor should be added to the loop filter. After the proper connection of all the components, the LF model looks like as in Figure 2-2.
2.3. Linear PLL Model and Transfer Functions

The CPLL is a time-varying network because of the switching activity. Hence, simple transfer function analysis is not directly applicable [2]. Due to the complexity of the analysis of time-varying networks, CPLL operation is treated as time-invariant with some approximations. The transfer function can be derived based on assumptions of small error (linearized loop) and small loop bandwidth as compared to the input frequency (continuous-time approximation) [2]. The CPLL of Figure 2-2 can be modeled as a linear system as shown in Figure 2-8. The PFD and CPC are combined in one component and a frequency divider is placed to divide the reference frequency.

![Figure 2-8: Linearized CPLL model](image)

The closed loop systems are generally analyzed in s-domain, where s is the Laplace-transform complex variable. Laplace operation transforms signals from time-domain to frequency-domain, where the signals are functions of complex angular frequency. Since in this domain, the input and output are phases; it is also referred as phase domain. The rest of the transfer function analysis will be done in phase domain.

The phase is considered as the integral of the frequency. If the gain of the oscillator is called \(K_{OSC}\), then the oscillator can be linearized as \(K_{OSC}/s\). The frequency dividers are simply modeled with \(1/N\) and \(1/P\), where \(N\) and \(P\) are the dividing factors. \(K_p\) is the gain of the PFD and is equal to \(Icp/2\pi\), where \(Icp\) is the charge pump current [2]. The loop filter model is represented with \(LF(s)\). With this knowledge, the open loop transfer function of the PLL model in Figure 2-8 can be calculated as

\[
H(s) = \frac{\theta_o}{\theta_e} = \frac{Icp}{2\pi} \cdot LF(s) \cdot \frac{K_{osc}}{s}. \quad (2.4)
\]
The closed loop transfer function is given by

\[
\frac{\theta_o}{\theta_i} = \frac{\frac{I_{cp}}{2\pi} K_{osc} Num(s)}{s \cdot Den(s) + \left(\frac{2\pi K_{osc}}{N}\right) Num(s)}
\]  

(2.5)

where \( Num(s) \) and \( Den(s) \) represent the numerator and denominator of the loop filter transfer function respectively.

2.4. PLL Order and Type

The PLL order is calculated by adding one to the number of poles of the loop filter. One is added to take into account the inherent pole of the oscillator at the origin. First order PLL is a type-1 PLL with a single open-loop pole at the origin [8]. In a first order PLL, LF(s) is a scalar. PLLs with two open-loop poles at the origin are of kind type-2. In higher order PLLs, the loop filter contains one or more capacitors to reduce the ripples on the controlling signal.

2.5. Performance Parameters

In this section, the parameters affecting the loop characteristics and the dynamic behavior of the PLL will be described.

2.5.1. Loop Bandwidth and Damping Factor

The loop bandwidth \( (\omega_n) \) and damping factor \( (\zeta) \) can be estimated from the closed-loop response of the PLL. The phase response of a second-order PLL is given by the ratio of output phase and input phase [3, 9]

\[
\frac{\theta_o}{\theta_i} = N \cdot \frac{1 + 2\zeta \cdot \left(\frac{s}{\omega_n}\right)}{1 + 2\zeta \cdot \left(\frac{s}{\omega_n}\right) + \left(\frac{s}{\omega_n}\right)^2}
\]  

(2.6)

where \( \zeta \) is given by

\[
\zeta = \frac{1}{2} \cdot \sqrt{\frac{1}{N} \cdot I_{cp} K_{osc} R_1^2 C_1}
\]  

(2.7)
and $\omega_n$ is given by

$$\omega_n = \frac{2\zeta}{R_1 C_1}.$$ (2.8)

The loop bandwidth is also referred as loop crossover frequency ($\omega_C$). The crossover frequency identifies the response rate of the PLL and the damping factor identifies the stability of the system [9]. In order to avoid instability, $\omega_C$ is generally chosen as 1/10 or 1/20 of the reference frequency. And typical values of $\zeta$ lie between 0.5 and 2, with 0.707 usually the preferred value [8].

### 2.5.2. Settling Time

When a change occurs in the reference frequency of the PLL, a number of cycles proportional to the magnitude of the change are required for the loop to stabilize. The total time required for stabilization is defined as the settling time. Loops with larger crossover frequency are faster and hence they have shorter settling time. The settling time alternates for different order PLLs; because, additional poles of the loop filter can likely increase the settling time [6]. For higher order systems, analytical calculation of settling time is very complicated. For instance, in [6], third order PLL settling time could be estimated by repeating simulations for several crossover frequencies ($\omega_C$).

### 2.5.3. Tracking Range

Suppose initially a PLL is locked, which means the input frequency and the divided output frequency are equal. If a jump occurs in the reference frequency, the loop can track this change only if the magnitude of the change is within a range. The tracking range limitations arise due to the nonlinear components and oscillation frequency range [5]. Tracking range is used to characterize the behavior of PLLs; and it is an important parameter in the analysis of wide tuning range PLLs, as well.

### 2.6. Third Order PLL

The PLL in Figure 2-8 is a third order PLL and will be analyzed in detail in this section.
2.6.1. Transfer Function

The impedance of the loop filter shown in Figure 2-9 is

\[ LF(s) = \frac{C_1}{C_1 + C_2} \cdot \frac{1}{sC_1} \cdot \frac{1 - s/z}{1 - s/p} \]  \hspace{1cm} (2.9)

where

\[ p = \frac{1}{-R_1 \frac{C_1C_2}{C_1 + C_2}} \] \hspace{1cm} (2.10)

and

\[ z = \frac{1}{-R_1C_1}. \] \hspace{1cm} (2.11)

If (2.9) is inserted into (2.4), the open loop transfer function is calculated as

\[ H_{\text{open}}(s) = \frac{s \left( \frac{Icp}{2\pi} K_{\text{OSC}} R_1 C_1 \right) + \frac{Icp}{2\pi} K_{\text{OSC}}}{s^3(C_1C_2R_1) + s^2(C_1 + C_2)}. \] \hspace{1cm} (2.12)
2.6.2. Frequency Response and Stability

The gain and phase of the open-loop transfer function (2.12) are plotted in Matlab [10] and are shown in Figure 2-10.

In Figure 2-10, $\omega_Z$ is the zero frequency and $\omega_C$ is the unity gain frequency. Since there are two open-loop poles at the origin, the phase starts at $-180^0$. The zero adds positive phase. At $\omega_C$, the phase margin is positive, hence the loop is stable. It can be pointed out that without a zero, stability cannot be achieved.

The stability is an important criterion for any PLL design. The critical parameters for stability analysis are phase margin (PM), damping factor and crossover frequency.

The phase margin of the third order PLL is

$$PM = \tan^{-1}(\tau\omega_C) - \tan^{-1}\frac{\tau\omega_C}{b + 1}$$

(2.13)

where $b = C_3/C_2$, $\tau = R_1C_1$ and $\omega_C$ is the crossover frequency. Maximum phase margin is achieved [6] when

$$\omega_C = \frac{\sqrt{b + 1}}{\tau}$$

(2.14)

and the corresponding phase margin in this case is given by

$$PM_{max} = \tan^{-1}(\sqrt{b + 1}) - \tan^{-1}\left(\frac{1}{\sqrt{b + 1}}\right).$$

(2.15)
The maximum phase margin is only a function of b. Hence, the ratio $C_1/C_2$ should be selected carefully to avoid instability. For all crossover frequencies, there is a minimum for the settling time when $PM \approx 50^0$ ($b \approx 6.5$) [6]. Therefore, PM of PLL applications should be selected close to 50 degrees.

To find the values of the parameters giving the maximum phase margin, (2.14) is forced and the following relation is get [6]:

$$\frac{Icp K_{OSC}}{2\pi N} \frac{b}{b + 1} = \frac{C_1}{\tau^2} \sqrt{b + 1}$$

(2.16)

As it is stated before, $\zeta$ should be selected as 0.707. Then, the values of the other parameters could be calculated using equations (2.7) and (2.8). Lastly, the crossover frequency $\omega_c$ is selected as 1/10 or 1/20 of the reference frequency in order to keep the continuous-time approximation valid.

### 2.7. Noise Analysis of PLL

PLL circuits are widely used in communication systems. Mainly, they take part in clock generation. The utilization of well-timed clocks is of critical importance in these systems. Any noise in a PLL system can alter the timing of the clock signal. Therefore, the performance of PLL in the existence of noise sources should be studied before the production.

#### 2.7.1. Noise Sources

There are two main factors that disturb the power-frequency spectrum of PLL output signal as shown in Figure 2-11 [11]. The first factor is random noise fluctuations due to device noise such as flicker noise, shot noise and thermal noise. It is named as phase noise. The second factor is spurs resulting from internal imperfections and mismatches in devices.

![Figure 2-11: Power-frequency spectrum of the output signal (11)](image)
2.7.2. Linear Phase Noise Model

Figure 2-12 depicts the linear phase noise model formed by adding the phase noise contributions of each sub-block.

\[ \theta_{\text{ref}} \text{ and } \theta_{\text{OUT}} \text{ are reference phase noise and PLL output phase noise, respectively. } I_{n,cp} \text{ is the current noise source inserted by PFD and CPC. } V_{n,lf} \text{ is the filter voltage noise source resulting from the resistor thermal noise. } \theta_{\text{OSC}} \text{ is oscillator output phase noise. Last phase noise component } \theta_{\text{DIV}} \text{ comes from the frequency divider.} \]

The two main noise sources are \( \theta_{\text{REF}} \) and \( \theta_{\text{OSC}} \). Because, in a careful design phase noise contributions of PFD/CP, loop filter and frequency divider are negligible [6]. Each noise source is shaped by noise transfer functions. The noise transfer function from \( \theta_{\text{REF}} \) to \( \theta_{\text{OUT}} \) is the same as the closed loop transfer function (2.5) and is a low pass function:

\[
\frac{\theta_{\text{OUT}}}{\theta_{\text{REF}}} = \frac{K_p K_{\text{OSC}} \text{Num}(s)}{s \cdot \text{Den}(s) + \left(\frac{K_p K_{\text{OSC}}}{N}\right) \text{Num}(s)} \quad (2.17)
\]

where \( \text{Num}(s) \) and \( \text{Den}(s) \) represent the numerator and denominator of the loop filter transfer function respectively.

On the other hand, oscillator noise is high pass filtered [6]:

\[
\frac{\theta_{\text{OUT}}}{\theta_{\text{OSC}}} = \frac{s \cdot \text{Den}(s)}{s \cdot \text{Den}(s) + \left(\frac{K_p K_{\text{OSC}}}{N}\right) \text{Num}(s)}. \quad (2.18)
\]

Therefore, at low frequencies the overall PLL noise is dominated by the reference phase noise whereas it is dominated by oscillator phase noise at high frequencies.
3. **Wide-Tuning Range CPLL**

In a wide-tuning range CPLL, the output frequency is modified whenever a change occurs in reference frequency ($f_{\text{REF}}$) or in the division ratio of the frequency dividers ($N$ or $P$). To keep optimal performance in the case of a change in these parameters, it is important to scale loop dynamics namely the loop bandwidth. In an adaptive-bandwidth PLL, the loop bandwidth scales with the operating frequency and maintains optimal performance of the PLL for all frequencies [12]. Hence, wide-tuning range CPLL is preferably designed by an adaptive-bandwidth PLL topology.

3.1. **Design Procedure of Wide-Tune PLLs**

According to stability analysis results demonstrated in section 2.6.2, the values of $\omega_c$, $\tau$, $b$ and $\zeta$ should be set properly. For this purpose, tuning of these parameters with respect to $f_{\text{REF}}$, $N$ and $P$ should be studied. Criteria for choosing $\omega_c$, $b$ and $\zeta$ have already been mentioned, but they will be revisited in this section. Another parameter to scale with respect to the input frequency and division ratio is the bias current of CPC.

The explanation of design process will start by choosing $\omega_c$. It is known that $\omega_c$ is chosen 10 to 20 times smaller than the input frequency. If the input-frequency-to-loop-bandwidth ratio is called $M_F$, then

$$\omega_c < \frac{2\pi f_P}{M_F}$$  \hfill (3.1)

where $f_P = f_{\text{REF}}/P$.

Next, the value of $\tau$ will be related to the input frequency. From equation (2.14)

$$\tau = \frac{\sqrt{b+1}}{\omega_c} = \frac{\sqrt{b+1}}{2\pi} M_F \frac{1}{f_P}.$$  \hfill (3.2)

Here, $M_F$ is a constant. Also, $b$ is a constant that is set according to phase margin requirements. Hence, the zero frequency only depends on the value of $f_P$.

Since, $C_1$ has a constant value; the resistor ($R_1$) of the loop filter should be tunable in order to scale $\tau$ according to (3.2). Therefore, the value of $R_1$ is calculated by

$$R_1 = \frac{\sqrt{b+1}}{2\pi} \cdot \frac{M_F P}{C_1 f_{\text{REF}}}.$$  \hfill (3.3)

According to this relation, $R_1$ should be proportional to $P$.

Lastly, charge pump current needs to be calculated. If the value of $\tau$ is inserted into (2.16), $I_{\text{CPC}}$ is found as:
\[ I_{CP} = 8\pi^3 C_1 \cdot \frac{\sqrt{b+1}}{b} \cdot \frac{1}{MF^2} \cdot \frac{1}{K_{OSC}} \cdot N \cdot \left( \frac{f_{REF}}{P} \right)^2. \] (3.4)

Equation (3.4) suggests that the charge pump current is proportional to \( N \) and inversely proportional to \( P^2 \). Therefore, a programmable charge pump circuitry is needed. Making \( I_{CP} \) inversely proportional to \( P^2 \) is difficult. The way to solve this problem is to use current-controlled oscillator instead of voltage-controlled oscillator [13]. In this case:

\[ K_{OSC} = \frac{\partial I_c}{\partial V_C} \cdot \frac{\partial f_{osc}}{\partial I_c} = G_m \cdot K_{CCO} \] (3.5)

where \( G_m \) is the transconductance of a transconductor stage.

Now, (3.4) can be rearranged as

\[ I_{CP} \cdot G_m = \left( 8\pi^3 C_1 \cdot \frac{\sqrt{b+1}}{b} \cdot \frac{1}{MF^2} \cdot \frac{1}{K_{CCO}} \cdot f_{REF}^2 \right) \cdot \frac{N}{P^2}. \] (3.6)

Defining a reference constant bias current, \( I_R \), the charge pump current requirements can be satisfied by choosing \( I_{CP} = N \cdot I_R / P \) and \( G_m = (I_R / P) / V_{char} \) where [13]:

\[ I_R^2 = 8\pi^3 C_1 \cdot \frac{\sqrt{b+1}}{b} \cdot \frac{1}{MF^2} \cdot \frac{1}{K_{CCO}} \cdot f_{REF}^2 \cdot V_{char}. \] (3.7)

For a single MOS transistor used as transconductance and biased in sub-threshold, \( V_{char} \) is equal to \( U_T \) (thermal voltage), and in strong inversion it is equal to \( V_{dsat} \) (gate overdrive voltage). According to (3.7), \( I_R \) and \( C_1 \) is chosen and the design process is completed.

### 3.2. Design Issues of Wide-Tune PLLs

An issue with wide tuning range PLLs is to satisfy the requirements of \( I_{CP} \) and \( G_m \) presented in the previous section. The requirements can be achieved by precisely setting the reference bias current, \( I_R \), with respect to the operation frequency. The circuit should track any change at input frequency \( (f_P) \) and tune the value of \( I_R \) appropriately. The class of PLLs in which this bias current is adjusted automatically with respect to the operation frequency is known as self-biased PLLs [3]. The other concern is to implement a scalable resistor value \( (R_1) \) proportional to \( P \). Another important problem is keeping \( M_F \) parameter constant when there is a sudden change in the value of \( P \) or \( N \).

Consider a sudden change in \( f_P \) from \( f_{PI} \) to \( f_{PI} - \Delta f_P \) as shown in Figure 3-1 (a) [13]. It will take some time to scale loop dynamics in order to track this modification. During this time interval, \( M_F \) will not be constant and will have a value smaller than its initial value. Since, the stability of PLL loop extensively depends on loop bandwidth, \( M_F \) ratio should not become smaller than a critical value. The critical value can change from design to design, but generally \( M_F \) needs to be greater than 10.
On the other hand, when $f_P$ increases from $f_{PI}$ to $f_{PI} + \Delta f_P$, there would be no stability issue. But, during the transition the loop bandwidth will be smaller than $(f_{PI} + \Delta f_P)/M_F$. Therefore, useful information at the output of PFD can be completely filtered by the loop filter as illustrated in Figure 3-1 (b). In such case, the loop may not be able to track the changes at the input frequency. Hence, under any circumstances the value of loop bandwidth should be higher than $|f_{DIV} - f_P|$. From this analysis, it is concluded that these two phenomena limit the change that can occur at $P$ or $N$ [13].

![Figure 3-1: (a) Loop bandwidth variation with respect to input frequency (b) Discarded PFD output component](image)
4. Circuit Design

The design methodology can be divided in two parts. The first part is the MATLAB Simulink [10] implementation of the proposed PLL topology. The other one is the transistor level design of the same topology. Before the details of these two parts, the proposed PLL topology should be explained.

4.1. Proposed PLL Topology

Figure 4-1 shows the proposed PLL topology. The circuit contains two dividers with dividing factors $N$ and $P$. They are programmable circuits with dividing ratios 1/2/4/8/16. Their outputs are selected by a multiplexer according to the values of signals $SEL_N$ and $SEL_P$. The PFD output is converted from SCL signal level to full swing CMOS levels by a SCL-to-CMOS converter [9] and it is applied to CPC. The charge pump current is scaled with respect to controlling current, $I_C$, and $N$. The output of CPC is the voltage signal ($V_C$) that is needed to control the oscillation frequency. In this topology, the loop filter is second order. Hence, the PLL is of type-2 and third order.

A current controlled oscillator is preferred to be used. Therefore, a transconductor is needed to convert the voltage control signal to current control signal ($I_C$) with a relation

$$I_C = G_m V_C.$$  \hspace{1cm} (4.1)

One of the aims of this project is to implement a power scalable PLL. Using sub-threshold source-coupled logic in the design can help to have this property. Hence, some of the sub-blocks such as PFD, ring oscillator and frequency divider are designed by STSCL gates.

Controlling current, $I_C$, is copied to several blocks to scale their bias current with respect to the operation condition. Also, it is applied to a replica bias circuit whose purpose is to generate bias voltages $V_{BN}$ and $V_{BP}$ for NMOS bias transistors and PMOS load transistors in STSCL gates.

The bulk-drain connected PMOS transistor of the loop filter serves as a resistor. Its resistance value can be tuned by $V_{BP}$ bias voltage. This way the requirements mentioned in section 3.1 are satisfied.
Figure 4-1: Proposed self-biased adaptive-bandwidth PLL topology
4.2. MATLAB Implementation

At first, the proposed PLL topology will be designed by using the Simulink toolbox of MATLAB in order to verify the correctness of the system behavior. This tool enables creation of mathematical models. Also, the simulation speed is very fast compared to Spice simulation; therefore some implementation parameters, like the capacitors of the loop filter, charge pump current scaling ratio and the replica bias speed will be calculated in this design environment.

4.2.1. Simulink Models of PLL Building Blocks

In this part, the corresponding MATLAB Simulink model of each sub-block will be explained. The models refer to time-domain representations of the components. Detailed representations of all Simulink models can be found in appendix A.

4.2.1.1. Phase/Frequency Detector Model

MATLAB has a built-in generic PLL model. The PFD model is taken from this model [10]. The model uses the state machine representation of Figure 2-6 (a).

4.2.1.2. Charge Pump Circuit Model

In Simulink model, SCL to CMOS converter is not needed. Therefore, the design continues with CPC. The charge pump model is implemented by using ‘Embedded MATLAB Function’ feature [10]. This feature enables writing codes in MATLAB. The embedded function model of this block accepts controlling current, $I_C$, the scaling ratio, $N$, and the PFD output as the inputs and calculates the output current from these values.

4.2.1.3. Loop Filter Model

The transfer function of the loop filter is given by the equations (2.9), (2.10) and (2.11). The generic PLL model offers an implementation of this transfer function. However, in that model the values of $C_1$, $C_2$ and $R_I$ are constant. Since, in adaptive-bandwidth topology, the value of filter resistor is updated during the operation; the loop filter model is also realized with an ‘Embedded MATLAB Function’.

Firstly, the s-domain transfer function is converted to time-domain by taking the inverse-Laplace transform of (2.9).
Equation (2.9) can be rearranged as
\[
\frac{Y(s)}{X(s)} = \frac{1 - s/z}{-(s^2/p)(C_1 + C_2) - s/p(C_1 + C_2)}
\]  
(4.2)

where \(X(s)\) and \(Y(s)\) are the input and output of the filter, respectively.

The inverse-Laplace of (4.2) is
\[
x(t) - \frac{1}{z} \frac{dx(t)}{dt} = -\frac{1}{p} (C_1 + C_2) \frac{dy(t)^2}{dt^2} - \frac{1}{p} (C_1 + C_2) \frac{dy(t)}{dt}.
\]  
(4.3)

In time-domain, first order derivative of a function is approximated by
\[
\frac{dx(t)}{dt} = \frac{x(t) - x(t - \Delta t)}{\Delta t}.
\]  
(4.4)

where \(\Delta t\) (in seconds) should be selected small enough for better accuracy.

On the other hand, second order derivative of a function is approximated by
\[
\frac{dy(t)^2}{dt^2} = \frac{y(t + \Delta t) - 2y(t) + y(t - \Delta t)}{\Delta t^2}.
\]  
(4.5)

In a real-time application, it is not possible to have a sample from future like \(y(t + \Delta t)\). Hence, the time variable \(t\) of equations (4.4) and (4.5) will be replaced by \(t - \Delta t\). Then, they will be inserted into 4.3 to obtain the final result as
\[
x(t - \Delta t) - \frac{1}{\Delta t} \left( x(t - \Delta t) - x(t - 2\Delta t) \right) - y(t - \Delta t) \left( \frac{A}{\Delta t} + \frac{2A(1)}{\Delta t^2} \right) - y(t - 2\Delta t) \left( \frac{(-1/p)A}{\Delta t^2} - \frac{A}{\Delta t} \right)
\]
\[
y(t) = \frac{(-1/p)A}{\Delta t^2}
\]  
(4.6)

where \(x(t-\Delta t)\) and \(y(t-\Delta t)\) are the delayed input and output signals, respectively. And, \(A = C_1 + C_2\).

The equation (4.6) implemented with ‘Embedded MATLAB Function’ is used as the model of the loop filter.

### 4.2.1.4. Transconductor Model

The model is simply the code representation of the transconductance value, \(G_m\), given by equation (3.7).
4.2.1.5. Current Controlled Ring Oscillator Model

Simulink has a ready oscillator model in which the free running frequency, oscillator sensitivity (gain) and the initial phase are defined. CCO is created by using this ready component.

4.2.1.6. Frequency Divider Model

The basic building block of the frequency divider is the divide-by-two circuit given by Figure 2-4. This block can be composed by using the D flip-flop model of Simulink. Then, a programmable divide by 1/2/4/8/16 circuit would be formed by cascading four divide-by-two circuits and selecting the output by a multiplexer.

4.2.2. Simulink Model of Complete PLL System

Figure 4-2 is the Simulink model of the complete PLL topology introduced in Figure 4-1.

The model of 'Filter Resistor' is added to create a tunable resistor. The voltage drop across the loop filter resistor is decided to be 200mV; and it is kept constant. When the controlling current, $I_C$, changes, it takes some time for the bias current across the resistor, $I_{SS}$, to adjust itself. Since, the replica bias circuit generating the resistor bias voltage, $V_{BP}$, contains an amplifier inside, it introduces a delay. This delay can be illustrated as a first order transfer function in time domain with a relation of
$y(t) = \frac{x(t) - \frac{y(t - \Delta t)}{p_{dom} \Delta t}}{1 - \frac{1}{p_{dom} \Delta t}} \quad (4.7)$

where $p_{dom}$ refers to the dominant pole frequency of the amplifier. Here, $x(t)$ and $y(t)$ represent the input and output signals, respectively.

The bias voltages of the devices inside the CCO are also generated by the replica bias. Therefore, ‘Replica Bias Delay’ model is added to present the delay in $I_C$ signal of the oscillator.

In a real PLL application, there will be a time difference between the generation of $I_C$ and the adjustment of charge pump current. The ‘Charge Pump Delay’ component is added to care for this delay.

In order to be able to change the values of divider ratios $N$ and $P$ during the simulation, two switches which can track the simulation time are placed after the frequency dividers.

Simulink design environment needs a well-defined initial condition to operate correctly. To create the initial inputs of ‘Adaptive Loop Filter’, two ‘Variable Transport Delay’ blocks are utilized.

### 4.2.3. Results

Table 4.1 embodies the values of the PLL parameters as chosen for the simulations.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$b$</td>
<td>5</td>
</tr>
<tr>
<td>MF</td>
<td>20</td>
</tr>
<tr>
<td>$\zeta$</td>
<td>0.707</td>
</tr>
<tr>
<td>$K_{CCO}$</td>
<td>$10^{13}$</td>
</tr>
<tr>
<td>$C_1$</td>
<td>10 pF</td>
</tr>
<tr>
<td>$C_2$</td>
<td>2 pF</td>
</tr>
</tbody>
</table>

Using the $K_{CCO}$ value as presented in Table 4-1 and taking the oscillator bias current range as 10pA to 200nA, the expected output frequency tuning range is found as 100Hz to 2MHz.

Figure 4-3 is the controlling signal, $I_C$, graphic when input frequency $f_p=500$KHz and $N=2$.

In this case, the output frequency is expected to be $f_{OUT} = f_p \times N = 1$MHz and the required magnitude of $I_C$ is $f_{OUT}/K_{CCO} = 10^{-7}$. The simulation result coincide with this value.
Figure 4-3: Controlling signal, $I_c$, when $f_P = 500$KHz and $N=2$

Figure 4-4 indicates the behavior when there is a jump at the value of $P$ from 2 to 4 with $f_{REF} = 1MHz$. The result presents that stability is achieved with a jump factor of 2.

Figure 4-4: Controlling signal, $I_c$, when $P$ jumps from 2 to 4 with $f_{REF} = 1MHz$ and $N=2$
Figure 4-5 represents the behavior when there is a jump at the value of $P$ from 1 to 8 with $f_{REF}=1MHz$. Here, the loop is able to achieve stability for a jump factor 8.

In this chapter, modeling of the proposed PLL topology in MATLAB Simulink design environment is demonstrated. The approaches for achieving scalable loop dynamics and for replicating real-time PLL performance have been successful. Although the model is still open to modifications and improvements, this part can be concluded by summarizing the initial performance results of the PLL in Table 4-2.

<table>
<thead>
<tr>
<th>Measured PLL Performance</th>
<th>500Hz-2MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Synthesized Frequencies</td>
<td>500Hz-2MHz</td>
</tr>
<tr>
<td>Controlling Current</td>
<td>50pA-200nA</td>
</tr>
<tr>
<td>Replica Bias Speed</td>
<td>$2 \times (f_P/MF)$</td>
</tr>
<tr>
<td>CPC Scaling Ratio</td>
<td>$N/(10 \sqrt{10})$</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>Adaptive</td>
</tr>
<tr>
<td>Loop Bandwidth</td>
<td>Adaptive</td>
</tr>
<tr>
<td>Max. Jump in $P$ value</td>
<td>16</td>
</tr>
</tbody>
</table>
4.3. Transistor Level Implementation

In this section, the aim is to explain the transistor level design process of self-biased adaptive bandwidth PLL topology of Figure 4-1. The parts, which consist of the frequency divider, the PFD and the CCO, will be designed by digital integrated circuit (IC) design principles. On the other hand, parts like SCL to CMOS converter, CPC and transconductor will be implemented mainly by analog IC design principles. Hence, the design process will be mixed-signal.

For the digital parts, sub-threshold source-coupled logic design method will be extensively used due to its advantages of low power consumption and circuit operation over a wide frequency range. Therefore; firstly, some background about STSCL method will be formed.

4.3.1. Introduction on Source-Coupled Logic

Source-coupled logic (SCL) is a design method that differs from conventional CMOS design. It is based on differential logic with a general architecture presented in Figure 4.6.

The structure of SCL gates are composed of three different parts:

- a current source that provides a bias current, $I_{bias}$, to the differential pair
- a switching network, composed of nMOS differential pairs, that steers the bias current to one of the output branches according to differential input logic levels
- two resistive loads to switch from current domain to voltage domain and to create the differential output voltage

![Figure 4-6: Architecture of a generic SCL gate](image)
The inputs and the outputs of a SCL gate are fully differential. When the bias current is steered to one of the output branches, there will be a voltage drop, equal to

$$\Delta V = R_{\text{load}} \times I_{\text{bias}},$$

across the resistor of that branch. On the other branch, the output will be pulled up to $V_{DD}$, since no current flows through its resistor. Hence, the voltage difference, $\Delta V$, is equal to the output voltage swing, $V_{SW}$. And, the differential output voltage $V_{od} = V_{op} - V_{on}$ will change its value between $V_{OH} = \Delta V$ and $V_{OL} = -\Delta V$.

In order to completely switch the differential pair of a gate in a next stage, the output voltage swing has to be sufficiently high. That is, $V_{SW} > \sqrt{2}V_{dssat}$ ($V_{dssat}$ is the drain-source overdrive voltage of input NMOS devices) when the device is biased in strong inversion and bigger than $4nU_T$ when the device is biased in sub-threshold where $U_T = kT/q$ is the thermal voltage and $n$ is the sub-threshold slope factor [14].

For STSCL family, the generic gate structure is the same as that of SCL family. But, the transistors of a STSCL gate are biased in sub-threshold region. By sub-$V_T$ biasing, the power consumption is minimized; since, the tail bias current can be selected as low as few nA or even few pA. On account of this advantage, for ultra-low-power applications, this design technique is commonly used. But, to obtain enough voltage swing at the output with such a low tail bias current levels, load resistances should be on the order hundreds of $M\Omega$ [1, 19]. In order to implement these resistances, with an acceptable layout area, a different load concept is used. That is a PMOS device where the drain of the device is connected to its bulk [1, 19]. This concept and its $I$-$V$ characteristics are shown below:

![Figure 4-7](image-url)

**Figure 4-7:** (a) Conventional pMOS load device, (b) proposed load device, (c) $I$-$V$ characteristics of the conventional pMOS load (dotted) in comparison to the proposed device (solid line) [1]
It is concluded from Figure 4.7 (c) that it is possible to achieve a finite and controllable differential resistance with this load concept only by using a single minimum sized PMOS device [1].

If the capacitance seen by $V_{OP}$ or $V_{ON}$ is equal to $C_L$, then the delay of a STSCL gate is

$$\tau_{STSCL} = \ln(2) \times \frac{V_{SW \cdot C_L}}{I_{bias}}.$$  \hspace{1cm} (4.9)

It is observed that delay is inversely proportional to bias current and it is independent of supply voltage.

It can be proved that the power consumption $P_{STSCL}$ is equal to [1]

$$P_{STSCL} = V_{dd_{STSCL}} \cdot I_{bias}.$$  \hspace{1cm} (4.10)

Another important parameter in the characterization of STSCL design is power-delay-product ($PDP$). From equations (4.9) and (4.10), $PDP$ is obtained

$$PDP_{STSCL} = \ln(2) \times V_{dd_{STSCL}} \cdot V_{SW \cdot C_L}.$$  \hspace{1cm} (4.11)

which is independent of the bias current. Therefore, the delay of a gate can be changed without modifying PDP, which is an advantage that is not available in conventional CMOS topologies [1].

### 4.3.2. Design of a Conventional STSCL Gate

The transistor model of a STSCL gate is drawn in Figure 4.8.
The sizing of the devices should be realized by paying attention to the needs of low power consumption, sufficient output voltage swing and minimized PDP product.

In this project, the circuits will be developed by a conventional 90nm CMOS process. The parameters used to size the devices are summarized in Appendix B.

### 4.3.2.1. Differential Pair

For low power consumption, it is essential to decrease the supply voltage value. It is possible to obtain minimal supply voltage by biasing the differential pair nMOS transistors in weak inversion, for which the drain-source voltage, $V_{DS,sat}$ is around $4U_T \approx 100mV$.

The weak inversion operation is enforced when the inversion factor $I_C$ is smaller than 0.1:

$$I_C = \frac{I_{bias}}{2n\beta U_T^2} = \frac{I_{bias}}{2nK_P \frac{W}{L} U_T^2} < 0.1$$  \hspace{1cm} (4.12)

In this PLL design, the bias current is expected to change from a few pA to a few hundreds of nA. Hence, the bias current range is selected as [10pA, 200nA]. The weak inversion should hold for any value in this range. The worst case condition occurs when $I_{bias}$ is largest ($I_{bias} = 200nA$). The sizing with respect to this constraint is:

$$\frac{W}{L} = \frac{I_{bias}}{2nK_P I_C U_T^2} > 2.4$$  \hspace{1cm} (4.13)

with the constraint of (4.13), the dimensions are chosen as $W=250nm$ and $L=90nm$.

### 4.3.2.2. Current Source

The current source is designed with a cascode current mirror, as proposed in Figure 4.9:

![Figure 4-9: Cascode current mirror](image)
The cascode device creates a high resistance at the output and it preserves the bottom transistor from variations in $V_{out}$. The bias voltage, $V_b$, and the output voltage, $V_{out}$, should be large enough to ensure the saturation of transistors T1 and T2, respectively. Operation in saturation will also improve the matching of $I_{REF}$ and $I_{OUT}$.

To ensure saturation region operation, $V_{out}$ should be greater than $V_{P1} + V_{P2}$ where, $V_{P1}$ and $V_{P2}$ are the pinch-off voltages of transistors T1 and T2. In order to minimize this sum, transistors T2 and T2’ are chosen of type low threshold voltage (LVT) NMOS.

For T1 to be in saturation, the condition is

$$V_{D1} > V_{P1} = \frac{V_b - V_{th1}}{n}. \hspace{1cm} (4.14)$$

And, the drain voltage of T1 is equal to

$$V_{D1} = V_b - V_{DS,sat2} = V_b - \sqrt{\frac{2I_{REF}}{n\beta_2}}. \hspace{1cm} (4.15)$$

If (4.15) is inserted into (4.16), then

$$\beta_2 > \frac{2I_{REF}}{(V_b - V_{P1})} \geq \frac{2I_{REF}}{(V_{th1}/n)^2}. \hspace{1cm} (4.16)$$

The dimensions are approximately chosen as $W_2=120nm$ and $L_2=500nm$.

For the transistor T1, the sizing is decided as $W_1=500nm$ and $L_1=4\mu m$. Here, the length is big to improve the matching. With the proposed width and length dimensions, the mismatch between the currents of two branches is around 78% when $I_{REF}=10pA$ and 1.78% when $I_{REF}=200nA$.

**4.3.2.3. Load Resistor**

The load resistor value is inversely proportional to the bias current as

$$R_L = \frac{V_{SW}}{I_{bias}}. \hspace{1cm} (4.17)$$

The voltage swing is generally selected as a few hundreds of mV in order to switch the differential pair of a next stage. A typical value is 200mV.

In this project, the tail bias current can lowered to the order of a few pA. With this level of bias current, the resistance should be very big to obtain enough swing. A conventional PMOS device can not be utilized, because the channel length required would be excessively big. Therefore, a bulk-drain connected PMOS load, explained previously in section 4.3.1, is preferred.
Using the EKV model, the output small signal resistance of the proposed load device in Figure 4.7 (b) is [15, 16]

\[
R_{SD} = \left( \frac{\partial I_{SD}}{\partial V_{SD}} \right)^{-1} = \left( \frac{n_p U_T}{I_b} \right) \left( (n_p - 1) e^{(n_p - 1) v_{SD}} + e^{-v_{SD}} \right)^{-1}
\]

(4.18)

in which \( v_{SD} = V_{SD}/n_p U_T \), \( I_b = I_0 e^{(V_{SG} - V_{TO})/n_p U_T} \) and \( I_0 = 2n_p \beta U_T^2 \).

It is possible to control the output resistance through \( V_{SG} \), hence through the current \( I_{SD} \). On account of the exponential relationship between \( R_{SD} \) and \( V_{SG} \), the resistance can be tuned in a very wide range.

For a high threshold voltage (HVT) PMOS device with dimensions of \( W=120\)nm and \( L=500\)nm, the following \( I-V \) characteristics of Figure 4-10 is obtained.

According to the simulation above, the current value can easily be put into the range 10pA to 200nA without resizing of the device.

Lastly, it should be noted that the voltage swing across the PMOS load should always be constant to get the correct adjustment of resistance with respect to bias current. This property will be obtained by using a replica bias circuit, which will be explained later in section 4.3.4.
4.3.3. Complexity of STSCL Gates

The number of stacked differential pairs placed in a STSCL gate defines the level (or the complexity). As the level of a gate increases, the number of functions which are possible to implement increases, as well. Also, since inverted and non-inverted outputs are available, and the negation of one input of a gate is achieved by switching the positive and negative ends of the differential signal, the function implemented by a gate can be varied in multiple ways [17]. Figure 4-11 shows generic 1-level and 2-level gates and the functions associated with them.

![Diagrams showing 1-level and 2-level generic STSCL gates](image)

Figure 4-11: 1-level and 2-level generic STSCL gates[17]

The functional variety of 2-level STSCL gate is enough for the purposes of this project. And, it is used as the basic building component of the following blocks: PFD, frequency divider and oscillator.

2-level STSCL gates used in this project are presented below Figure 4.12.

As the function of Figure 4.12 (b) has two inputs, the third differential pair is unnecessary. However, it is not completely removed; but rather replaced by a single NMOS transistor with its gate connected to Vdd. This scheme is preferred in order to keep the logic path length the same for all possible input configurations.
4.3.4. Periphery Circuits for STSCL

4.3.4.1. Replica Bias

As it is pointed out before, the voltage swing across the pMOS load should always be kept constant by the aid of a replica bias circuit. 1-level SCL gate with its replica bias (RB) circuit is figured below:

Figure 4-13: 1-level SCL gate with its replica bias circuit [1]
The amplifier, which is generally of type operational transconductance amplifier (OTA), acts as a voltage follower and generates the output voltage swing that has a fixed value defined by \( V_{DD} - V_{REF} \). The output of RB circuit, \( V_{BP} \), is used to tune the pMOS load resistances of all STSCL gates. A precise off-chip current, \( I_{SS} \), is mirrored to whole STSCL gates through current mirror bias, \( V_{BN} \). In order to obtain accurate biasing conditions, it is crucial to match RB to STSCL gates.

### 4.3.4.2. The Folded Cascode OTA

The amplifier of Figure 4.13 should have high gain, large enough phase margin to ensure stability, and low power consumption. These needs can be satisfied by a *Folded Cascode OTA* topology illustrated in Figure 4.14.

The sizing of the devices are realized with \( I_{OTA} = 10nA, V_{DD} = 1V, A_0 > 60dB \) and \( PM > 60^0 \). The dimensions can be found in Table 4-3.

![Figure 4-14: Folded-Cascode OTA topology](image)

<table>
<thead>
<tr>
<th>Device Name</th>
<th>Width W</th>
<th>Length L</th>
</tr>
</thead>
<tbody>
<tr>
<td>( P1 )</td>
<td>( 1\mu ) m</td>
<td>( 250nm )</td>
</tr>
<tr>
<td>( P2 )</td>
<td>( 1\mu ) m</td>
<td>( 250nm )</td>
</tr>
<tr>
<td>( N1 )</td>
<td>( 500nm )</td>
<td>( 120nm )</td>
</tr>
<tr>
<td>( N2 )</td>
<td>( 1\mu ) m</td>
<td>( 500nm )</td>
</tr>
<tr>
<td>( N3 )</td>
<td>( 1\mu ) m</td>
<td>( 500nm )</td>
</tr>
</tbody>
</table>
4.3.5. Proposed Topologies of PLL Building Blocks

4.3.5.1. Phase/Frequency Detector

During the implementation, the PFD model of Figure 2-6 is modified as represented in Figure 4.15.

The inverters in the reset path are added to eliminate the dead zone of the charge pump [6]. The inverters and the AND gate are implemented with 2-level STSCL topologies of Figure 4.12. For correct charge pump behavior, the inverted \( UB \) and \( DB \) signals are needed; and they should be applied at the same time as the non-inverted ones to avoid mismatches. Therefore, an output stage consisting of CMOS inverters and CMOS transmission gates (TG) are added to the basic PFD model. TG delay is matched to the delay of an inverter to create both \( U-UB \) and \( D-DB \) at the same time.

Figure 4.15 also contains a detailed view of the D flip-flop. The master and slave latches of the flip-flop are resettable. Their corresponding STSCL circuit schematic and an example simulation result of PFD are drawn below:
Figure 4-16: STSCL latch circuit schematic

Figure 4-17: Up, Down, Reset signals from PFD simulation
4.3.5.2. SCL-to-CMOS Converter

The PFD has differential outputs, whereas the inputs of the CPC are rail-to-rail swing that is they swing between supply and ground. To overcome this incompatibility, an interface called SCL-to-CMOS converter is needed. This interface behaves like a level shifter and its circuit schematic is shown in Figure 4.18.

The level shifter is a comparator which compares two analog input signals \( V_{IP} \) and \( V_{IN} \). The circuit consists of two amplifier stages; and its bias current is supplied by a cascode current mirror. The first amplifier stage is an OTA. Since, OTA gain is relatively low, a second amplifier stage, an inverter, is added to enhance the gain. It is vital to have high enough gain to saturate the output to one of the supply levels.

![Figure 4-18: SCL-to-CMOS converter](image)

The type of the differential pair NMOS transistors \((N1)\) is high threshold voltage (HVT) to be able to completely close the transistors on time at all input frequencies.

The transistors of the inverter are sized such that the low-to-high and high-to-low transitions take the same amount of time. The dimensions are summarized in Table 4-4.
Table 4-4: Transistor dimensions of the SCL-to-CMOS converter

<table>
<thead>
<tr>
<th>Device Name</th>
<th>Width W</th>
<th>Length L</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1</td>
<td>1µm</td>
<td>250nm</td>
</tr>
<tr>
<td>N1 (HVT)</td>
<td>500nm</td>
<td>150nm</td>
</tr>
<tr>
<td>P2</td>
<td>2µm</td>
<td>90nm</td>
</tr>
<tr>
<td>N2</td>
<td>1µm</td>
<td>90nm</td>
</tr>
</tbody>
</table>

Figure 4.19 proves the conversion of differential input signal to full swing single-ended output signal.

4.3.5.3. Charge Pump and Loop Filter

The CPC used in this project is based on the topology explained in [6]. The circuit diagram is shown in Figure 4.20.

This topology is preferred due to its capability of keeping the mismatch between $I_{UP}$ and $I_{DOWN}$ currents low. This is achieved by a Feedback Network comparing the single-ended output, $O_P$, with the voltage of the replica bias, $V_r$. 
The continuously on $I_{UP}$ and $I_{DOWN}$ currents are steered to one of the branches of the Charge Pump by the aid of switch transistors N1-N2 and P1-P2. On the other hand, the transistors N3-N4 and N5-N6 are used to reduce the charge injection into the oscillator control line by the $U$ and $D$ signals [6]. Lastly, to prevent node $O_N$ from drifting to the rails when neither of the $U$ and $D$ signals is active, a rail to rail unity gain buffer of the kind shown in Figure 4-211 is placed between the two output nodes [6].

![Charge Pump Circuit Diagram]

**Figure 4-20:** Charge pump circuit

<table>
<thead>
<tr>
<th>Device Name</th>
<th>Width W</th>
<th>Length L</th>
</tr>
</thead>
<tbody>
<tr>
<td>$W_p$</td>
<td>2µm</td>
<td>1µm</td>
</tr>
<tr>
<td>P1-P4</td>
<td>1µm</td>
<td>250nm</td>
</tr>
<tr>
<td>N1-N4</td>
<td>500nm</td>
<td>500nm</td>
</tr>
<tr>
<td>N5</td>
<td>500nm</td>
<td>100nm</td>
</tr>
<tr>
<td>P5</td>
<td>1µm</td>
<td>100nm</td>
</tr>
</tbody>
</table>

Table 4-5: Transistor dimensions for charge pump circuit
The dimensions of \( W_n \) is intentionally not provided. Because, instead of a single NMOS bias transistor, the cascode current mirror from section 4.3.2.2 is used.

![Figure 4-21: Rail-to-rail unity gain buffer [6]](image)

<table>
<thead>
<tr>
<th>Device Name</th>
<th>Width W</th>
<th>Length L</th>
</tr>
</thead>
<tbody>
<tr>
<td>( N1 )</td>
<td>2µm</td>
<td>250nm</td>
</tr>
<tr>
<td>( P1 )</td>
<td>2.25µm</td>
<td>500nm</td>
</tr>
<tr>
<td>( N2 )</td>
<td>1.5µm</td>
<td>1µm</td>
</tr>
<tr>
<td>( P2 )</td>
<td>2µm</td>
<td>2µm</td>
</tr>
</tbody>
</table>

According to Table 4-7, the percentage mismatch between the currents \( I_{\text{UP}} \) and \( I_{\text{DOWN}} \) smaller than 0.3% for the current range of interest. As the bias current increases, the mismatch decreases.

<table>
<thead>
<tr>
<th>Bias Current</th>
<th>( I_{\text{UP}} )</th>
<th>( I_{\text{DOWN}} )</th>
<th>Mismatch (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100pA</td>
<td>108.989 pA</td>
<td>108.74 pA</td>
<td>0.23</td>
</tr>
<tr>
<td>1nA</td>
<td>1.02987 nA</td>
<td>1.02775 nA</td>
<td>0.21</td>
</tr>
<tr>
<td>10nA</td>
<td>10.1719 nA</td>
<td>10.1582 nA</td>
<td>0.13</td>
</tr>
<tr>
<td>100nA</td>
<td>101.129 nA</td>
<td>101.09 nA</td>
<td>0.03</td>
</tr>
<tr>
<td>200nA</td>
<td>201.883 nA</td>
<td>201.809 nA</td>
<td>0.03</td>
</tr>
</tbody>
</table>

The loop filter given in Figure 4-1 is kept the same for transistor level design.
### 4.3.5.4. Transconductor

Transconductor is a key component that converts the voltage control signal to current control signal. This component has to offer wide output current swing and should meet the loop stability requirements. It should have a wide output current range; since, this range is supposed to cover the whole bias current range of the oscillator. On the other hand, the adjustment of its transconductance with respect to operation condition should satisfy the loop stability requirements.

The proposed transconductor [13] consists of a single PMOS device and a resistor. For compatibility with the rest of the circuit design, the resistor is implemented with a bulk-drain connected PMOS device.

For a PMOS device biased in weak inversion the transconductance ($G_m$) is equal to

$$G_m = \frac{I_{OUT}}{nU_T}.$$ 

The purpose of the local swing control loop is to keep the voltage swing, $V_{SW}$, across the resistor at a constant value of $V_{DD} - V_{REF}$ and hence to enable resistivity tuning in a wide range. The amplifier of the swing control loop, $A_V$, is realized with the folded cascode OTA of the replica bias. The current source M7-M8 is implemented with the cascode mirror of STSCL gates.

Based on simulation results the circuit can provide output current swing between 30pA to 190nA.

![Figure 4-22: Wide swing transconductor [13]](image-url)
The current-controlled ring oscillator is composed of delay cells. Each delay stage is identical and designed with STSCL topology. The cells are 2-level STSCL gates which are configured as inverters. As opposed to CMOS based ring oscillators, the number of delay cells can be even as well as odd; since, the input and output signals are differential.

According to scheme above, the bias voltages of NMOS bias transistor and PMOS load inside each delay cell are generated by the replica bias circuit. This circuit properly adjusts the bias voltages with respect to controlling current.

An output buffer is used to connect the oscillator output to the frequency divider circuit without disturbing the performance of the oscillator [13].
The performance results of Figure 4-25 indicate that the oscillation frequency ranges from about 700Hz to 21MHz for a bias current range of 10pA to 1µA.

The calculations for delay at each stage and oscillator gain can be found in appendix C.

![Figure 4-25: Simulated tuning range of CCO with 8 delay elements](image)

### 4.3.5.6. Frequency Divider and Multiplexer

Design of frequency divider and multiplexer are both based on STSCL topology. The topologies are detailed in Figure 4-26.
The frequency divider is composed as a programmable divide by 1/2/4/8/16 circuit. The D flip-flops inside the divide-by-two circuits are constructed with STSCL latches. The correct output is chosen by the multiplexer with respect to the values of the select signals, \( SEL_N \) or \( SEL_P \). These select signals are generated by conventional CMOS decoders.

### 4.3.6. Results

The proposed PLL has been implemented in a conventional 90nm CMOS technology. Table 4-8 summarizes the measured PLL performance in Cadence environment. Figure 4-27 shows transient response of PLL for two different operation conditions.

![Figure 4-26: (a) 5-to-1 Multiplexer, (b) Divide-by-two circuit](image)

Table 4-8: Measured PLL performance in Cadence environment

<table>
<thead>
<tr>
<th>Measured PLL Performance</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Synthesized Frequencies</strong></td>
<td>32KHz-3.2MHz</td>
</tr>
<tr>
<td><strong>Controlling Current</strong></td>
<td>1.35nA-142.7nA</td>
</tr>
<tr>
<td><strong>Phase Margin</strong></td>
<td>45.4°</td>
</tr>
<tr>
<td><strong>Kcco</strong></td>
<td>2.2x10^{14}</td>
</tr>
<tr>
<td><strong>C_1</strong></td>
<td>10 pF</td>
</tr>
<tr>
<td><strong>C_2</strong></td>
<td>2 pF</td>
</tr>
<tr>
<td><strong>Max. Jump in P value</strong></td>
<td>100</td>
</tr>
</tbody>
</table>
Figure 4-27: Controlling signals, fref=1MHz and N=4 (a) when P jumps from 2 to 4 (b) when P jumps from 2 to 16
Power consumption measurements show that it is possible to scale power with respect to operation frequency. The scaling behavior can be observed from Figure 4.28.

![Figure 4-28: Scalable power consumption](image)

5. **Conclusion**

5.1. **Achievements**

After acquiring background knowledge about PLL design and STSCL, the challenge of implementing widely adjustable and low power clock generators is targeted. A self-biased and adaptive-bandwidth PLL topology is proposed as a solution to this challenge.

At system level analysis, the possible values for performance parameters of a real-time PLL such as phase margin requirement, replica bias delay and input-frequency-to-loop-bandwidth ratio, are derived by using MATLAB Simulink design environment. Then, the circuit topologies of frequency divider, SCL-to-CMOS converter, charge pump, loop filter, transconductor and ring oscillator have been proposed and are developed in 90nm CMOS technology. Each component is tested individually and the correct functionalities are demonstrated. Compatibility to STSCL circuits and also scalable loop dynamics namely adjustable charge pump current and tunable loop filter resistance are obtained.

Lastly, the complete transistor level PLL is simulated and the output frequency range is found as 3.2KHz – 3.2MHz. The circuit power consumption is 4.47pW/Hz and allowable jump ratio for $P$ is found to be 100.
5.2. Future Work

The Simulink model of the proposed PLL topology should be revised to decrease the simulation time needed to get the final results. Also, more research should be done about the problems related to the sudden jumps in the value of divider ratio $P$; and the maximum allowable jump factor in the value of $P$ should be precisely found.

The output frequency range is calculations should be completed. Then, the power consumption of the PLL at the extreme frequencies of the swing range needs to be characterized. The transistor level design utilizes current mirrors, whose purposes are to copy the scaling current to sub-blocks. These blocks have large number of transistors. Therefore, an optimal design should be obtained for them in order to save from area. Lastly, after finishing all of the characterizations, the layout of the PLL needs to be drawn.

Lausanne, January 15, 2010

Hasene Gülperi Özsema
6. Bibliography


13. Tajalli, A. Power-Performance Scalable Circuit Design Using Subthreshold MOS. *PHD Dissertation*. 2010,


A. MATLAB Simulink Models

In figure A.1, the three states of PFD state machine can be seen. Here, s represents the output. Its value is equal to the difference $Up-Down$.

The complete PFD model is shown in figure A.2.

Figure A.3 is the charge pump circuit model. A switch is put to be able to change the value of divider ratio $N$ during the simulations.
The following lines form the *Embedded MATLAB Function* of the charge pump shown in figure A.3.

```matlab
function CPout = CP(input, Ic, N)
Icpc = (N*Ic)*(0.097);
CPout = (input*Icpc);
```

The loop filter with scalable resistor is represented in figure A.4. The memory units are added to obtain the delayed input and output signals.
The ‘Embedded MATLAB Function’ of the loop filter is given by:

```matlab
function output=loopfilter (delta,R1,C1,C2,inpdel1,inpdel2,outdel1,outdel2)
A=C1+C2;
zero=R1*C1;
pole=(R1*C1*C2)/A;

x=(pole*A)/(delta*delta);
coefoutdel1=(A/delta)-(2*x);
coefoutdel2=(x)-(A/delta);
inptout=inpdel1+zero*((inpdel1-inpdel2)/delta);
output=(inptout-(outdel1*coefoutdel1)-(outdel2*coefoutdel2))/x;
```

Figure A.6-4: MATLAB Simulink model of loop filter
The transconductor of the PLL is given in figure A.5:

A switch is added to make the value of $P$ changeable during the simulations as in the model of charge pump circuit.

The ‘Embedded MATLAB Function’ of the loop filter is written as:

```matlab
function Ic=Gm(Vc,P,C1,b,MF,Kcco,fref)

Ut=0.026;
x=8*(pi^3)*C1*((sqrt(b+1))/b)*(1/(MF^2))*(1/Kcco)*(fref^2)*Ut;
Ir=sqrt(x);
Gm=Ir/(P*Ut);
Ic=(Vc*Gm);
```

The oscillator component of MATLAB can be seen in figure A.6:
The specifications of this component are shown in figure below:

![Continuous-Time VCO (mask) (link)](image)

Generate a continuous-time output signal whose frequency changes in response to the amplitude variations of the input signal. The input signal must be a sample-based scalar.

**Parameters**

- **Output amplitude (V):**
- **Quiescent frequency (Hz):**
- **Input sensitivity (Hz/V):** $1e12$
- **Initial phase (rad):**

![Figure A.6-7: Specifications of oscillator component of MATLAB Simulink](image)

The divide-by-two circuit is designed as figure A.8:

![Figure A.6-8: MATLAB Simulink model of divide-by-two circuit](image)

D flip-flop in figure A.8 is a ready component of MATLAB. It has a clear input $CLR$. This port is not needed for the purposes of this project; therefore, it is set as a constant.
The frequency divider is created by cascading for divide-by-two circuits as represented in figure A.9:

Figure A.6-9: MATLAB Simulink model of frequency divider

In order to implement a scalable resistor, an additional block illustrated in figure A.10 is used:

Figure A.6-10: MATLAB Simulink model of scalable loop filter resistor

In case of a zero or negative controlling current, $I_C$, circuit operation may fail. Hence, a function called ‘Negative/Zero $I_C$ Handle’ is written:

```matlab
function Iout = CalcIout(Ic)
if (Ic<0)
    Iout = -(Ic);
elseif (Ic==0)
    Iout = 1e-15;
else
    Iout = Ic;
end;
```

The transfer function from controlling current $I_C$ to $I_{SS}$ is implemented with following code lines:
function Iss = IinToIssTransferFcn (delta, poledelay, Iin, outdel1)
pole = 2 * (3.14) * poledelay;
A = 1 / pole;
coefoutdel1 = A / delta;
Iss = (Iin + outdel1 * coefoutdel1) / (1 + (A / delta));

The delay due to the replica bias circuit is modeled like figure A.11:

![Figure A.6-11: MATLAB Simulink model of replica bias delay](image)

The transfer function from controlling current $I_c$ to $I_{cco}$ is implemented with following code lines:

function Icco = IcToIoscTransferFcn (delta, poledelay, Iin, outdel1)
pole = 2 * (3.14) * poledelay;
A = 1 / pole;
coefoutdel1 = A / delta;
Icco = (Iin + outdel1 * coefoutdel1) / (1 + (A / delta));
Lastly, the charge pump delay model can be seen in figure A.12. In a transistor level PLL, the charge pump current will be scaled by the help of a current mirror (CM). Usually, CMs are very fast. Therefore, the pole frequency value of the CM is selected big. The written code is the same as the code of the transfer function from $I_C$ to $I_{CCO}$ given above.

![Figure A.6-12: Charge pump delay model](image-url)
B. UMC 90nm Process Parameters

<table>
<thead>
<tr>
<th>N_12_LL</th>
<th>P_12_LL</th>
<th>N_12_LLVT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{OX}$</td>
<td>2.95E-09 [m]</td>
<td>$t_{OX}$</td>
</tr>
<tr>
<td>$C_{OX}$</td>
<td>12E-03 [F/m²]</td>
<td>$C_{OX}$</td>
</tr>
<tr>
<td>$V_T$</td>
<td>0.45 [V]</td>
<td>$V_T$</td>
</tr>
<tr>
<td>$\mu_0$</td>
<td>12.3E-03 [cm²/Vs]</td>
<td>$\mu_0$</td>
</tr>
<tr>
<td>$n$</td>
<td>1.2</td>
<td>$n$</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>N_12_LLHVT</th>
<th>P_12_LLHVT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{OX}$</td>
<td>2.95E-09 [m]</td>
</tr>
<tr>
<td>$C_{OX}$</td>
<td>12E-03 [F/m²]</td>
</tr>
<tr>
<td>$V_T$</td>
<td>0.53 [V]</td>
</tr>
<tr>
<td>$\mu_0$</td>
<td>28.2E-03 [cm²/Vs]</td>
</tr>
<tr>
<td>$n$</td>
<td>1.2</td>
</tr>
</tbody>
</table>

Thermal voltage: $U_T = \frac{kr}{q} \approx 26mV$ (at room temperature)

Inversion factor: $I_C = \frac{I_D}{2n\beta U_T^2}$

Parameter $\beta$: $\beta = \mu_0 C_{OX} \frac{W}{L} = K_p \frac{W}{L}$

The value of the sub-threshold slope factor, $n$, was changing from one bias condition or sizing to another one. Therefore, for all types, it is assumed as 1.2. The results obtained with this value were satisfying.
C. STSCL Gate Delay and Oscillator Gain

The delay of a STSCL gate is given by equation (4.9) as:

\[ \tau_p = \ln(2) \times \frac{V_{SW} \cdot C_L}{I_{bias}}. \]

And the frequency of the oscillator is:

\[ f_{osc} = \frac{1}{2.8 \cdot \tau_p} \]

where \( N \) is the number of stages.

The gain (sensitivity) of the current-controlled ring oscillator is given by

\[ K_{CCO} = \frac{I_{bias}}{\ln(2) \cdot V_{SW} \cdot C_L \cdot 2 \cdot N}. \]

If the load capacitance is assumed as 20fF, for bias current of 1A, the gain of the oscillator is found as:

\[ K_{CCO} = \frac{1}{\ln(2) \cdot (0.2) \cdot (20 \times 10^{-15}) \cdot 2.8} = 2.25 \times 10^{13}. \]